

LCFC Confidential


DG42A/DG52AMB Schematics Document

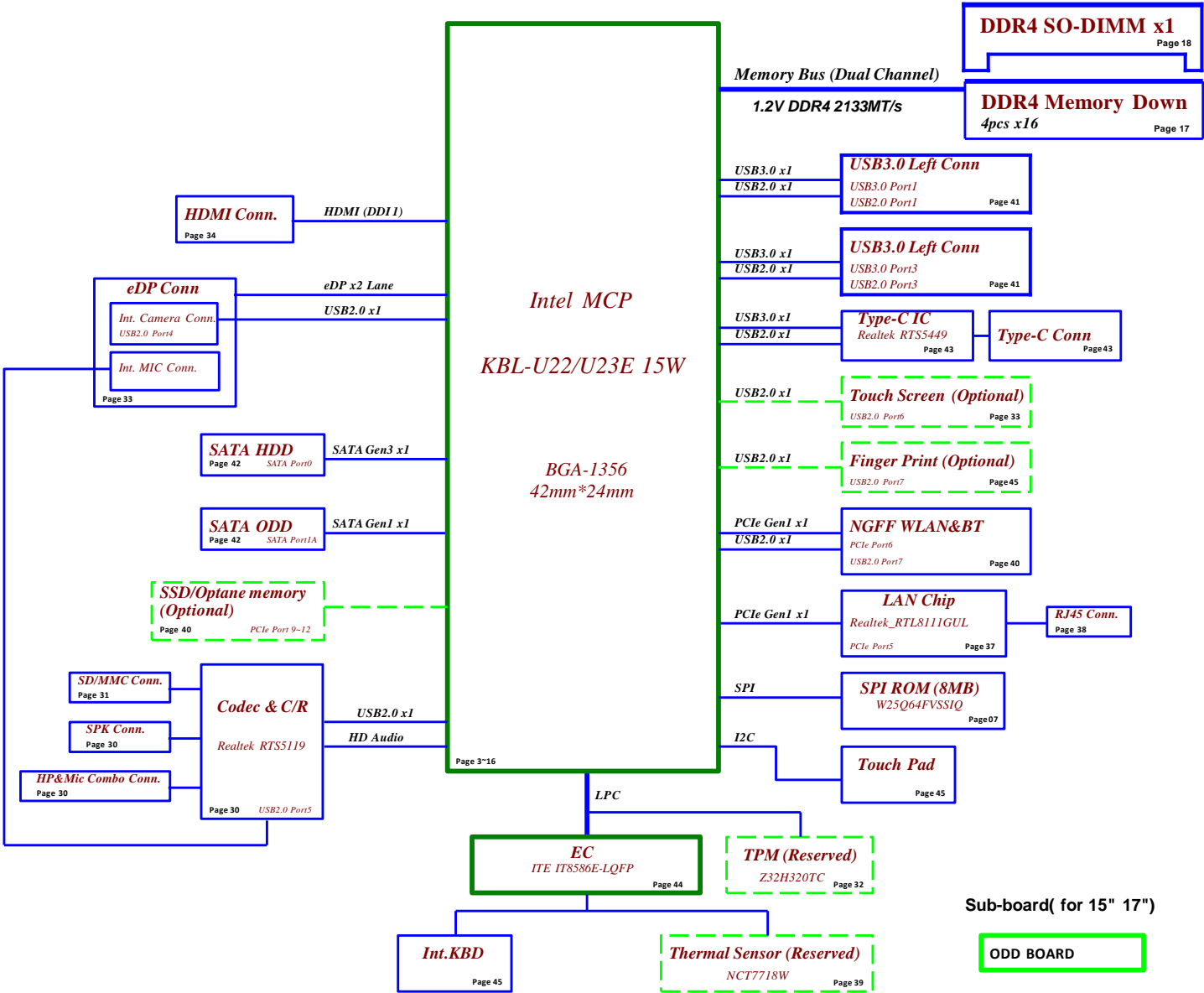
Kabylake-U22/U23E with DDR4

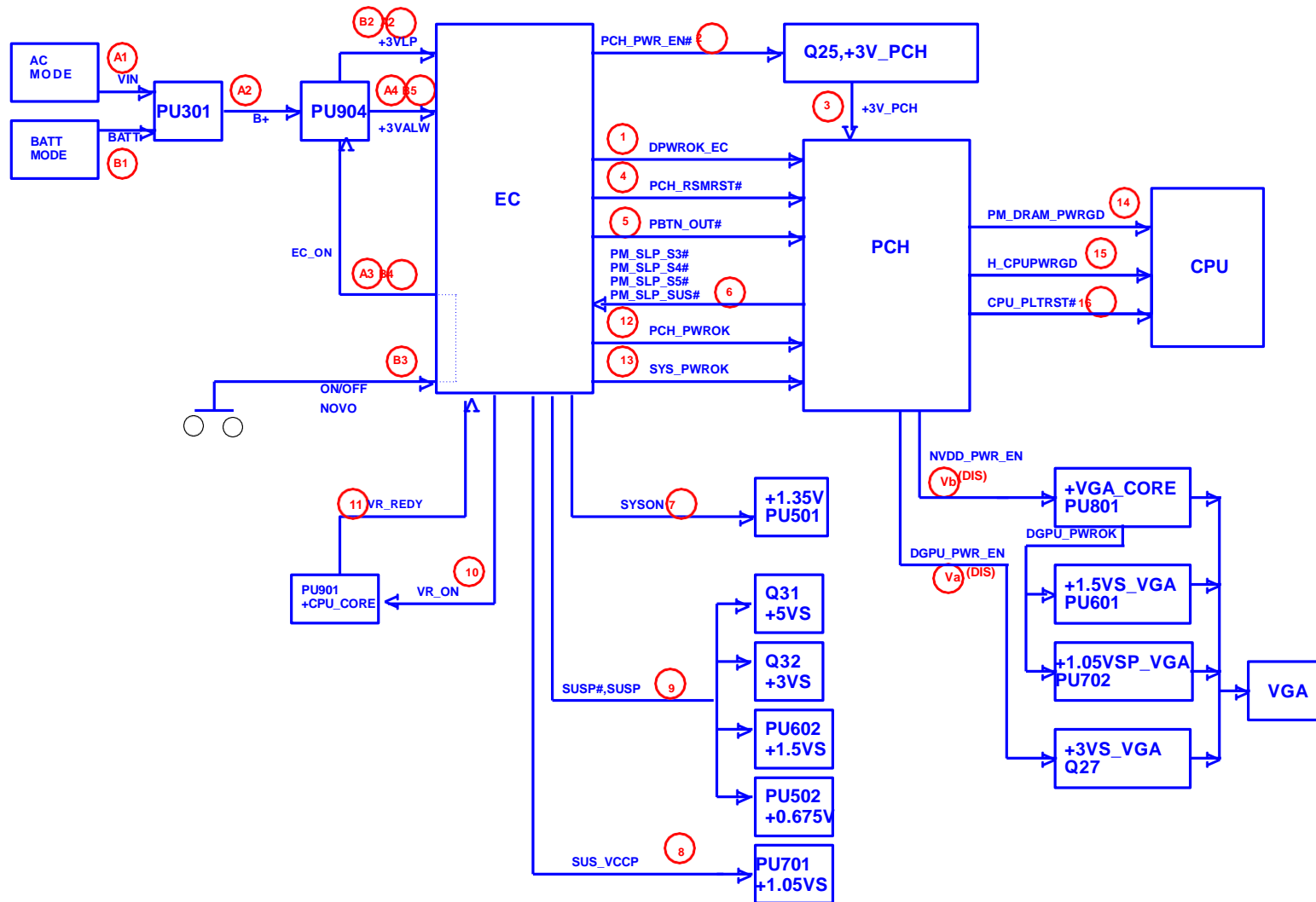
2017-01-19

REV:1.0


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Custom		DG42A		1.0	
Date:		Sunday, January 22, 2017		Sheet 1 of 60	

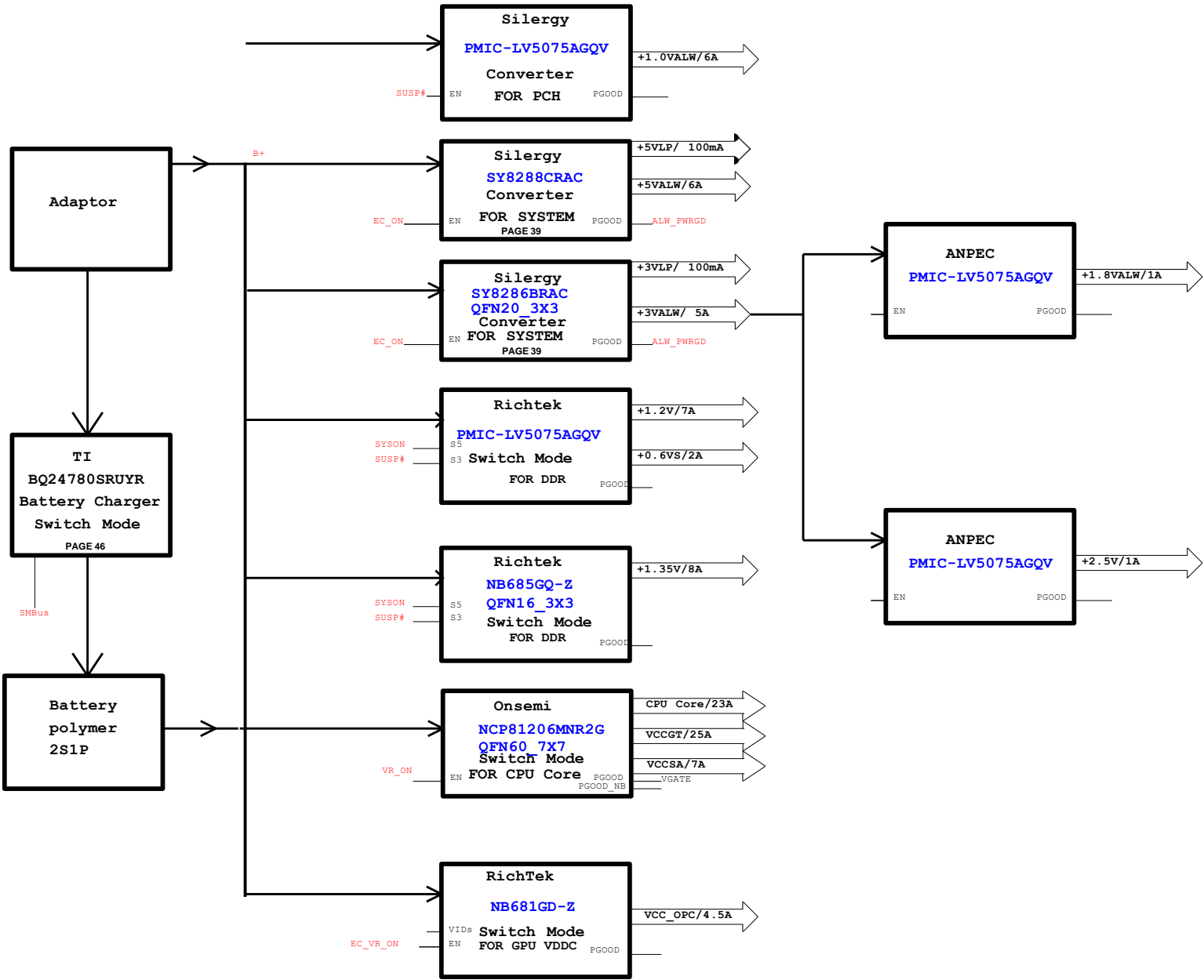






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Title	Power sequence block		
Size/Document Number	Custom	DG42A	
Date:	Sunday, January 22, 2017	Sheet	47 of 60



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1-4 X4 PCIE DGPU
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9-12 X4 PCIE Optane Memory
SATA	0 HDD
	1A ODD
	1B used as PCIE
	2 used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C oost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAM rank part
DUALRANK@	For dual VRAM rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

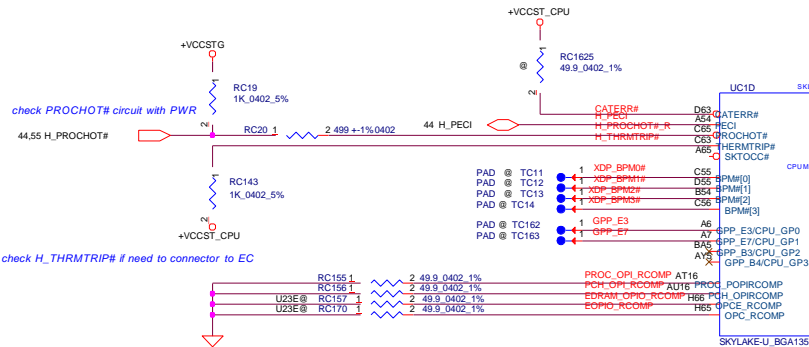
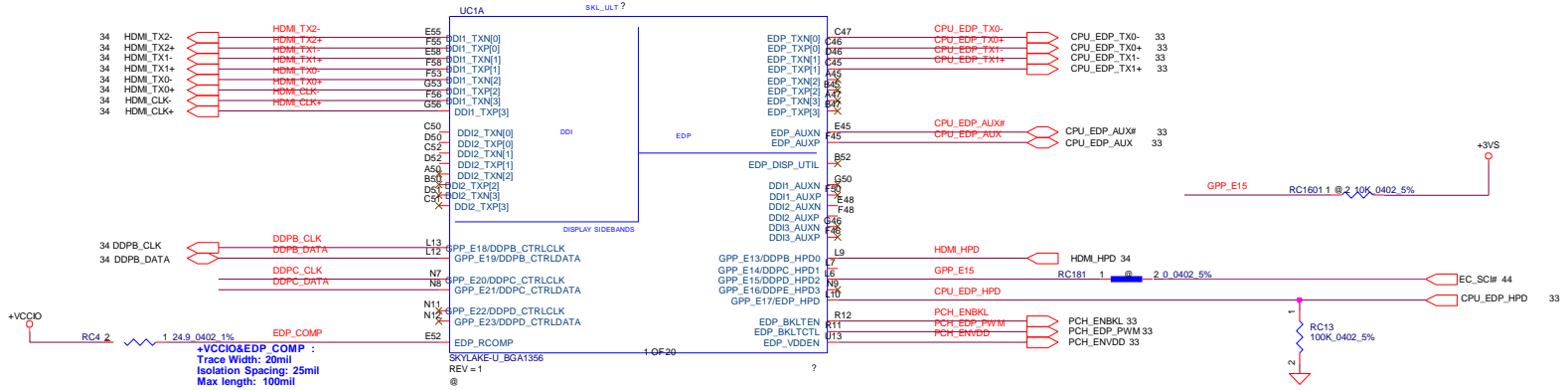
Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

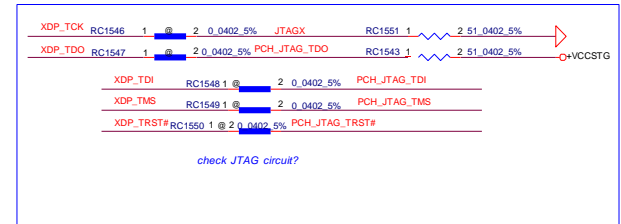
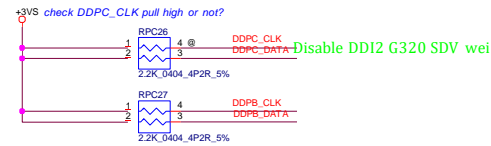
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					Document Number DG42A
					Date: Sunday, January 22, 2017 Sheet 3 of 60

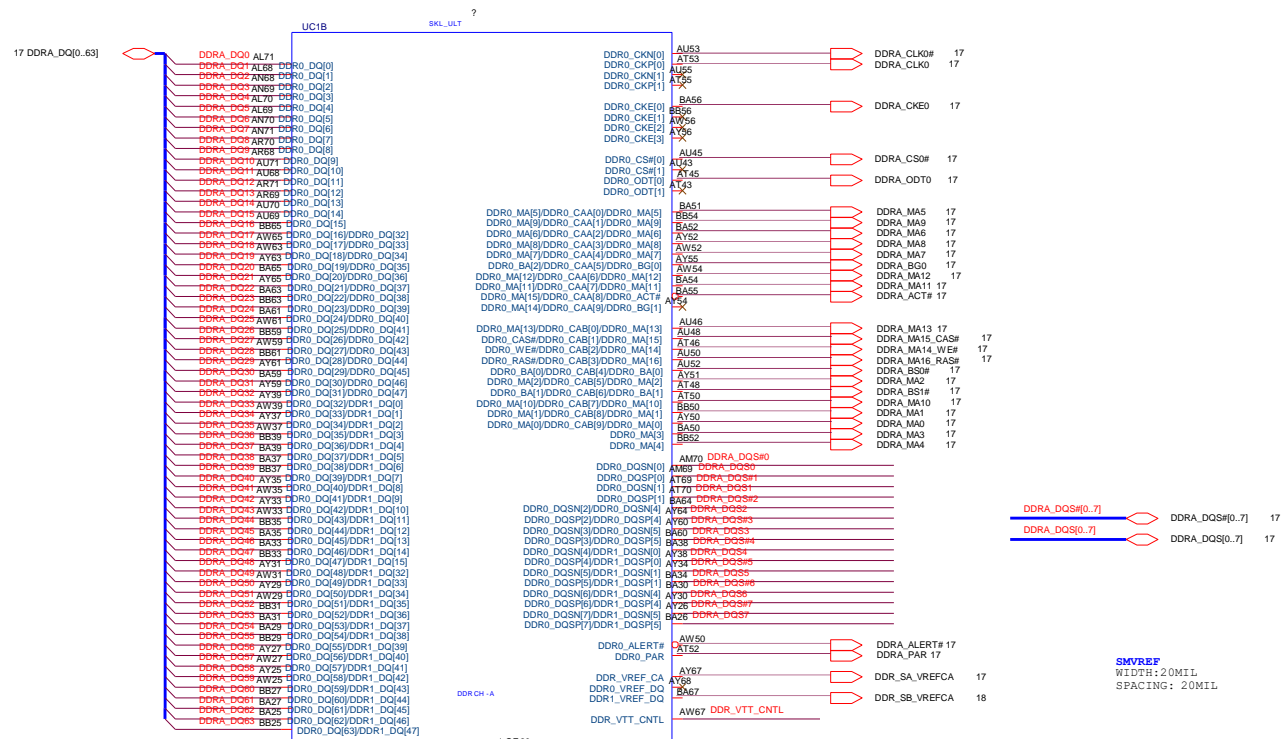
HDMI D2
HDMI D1
HDMI D0
HDMI CLK



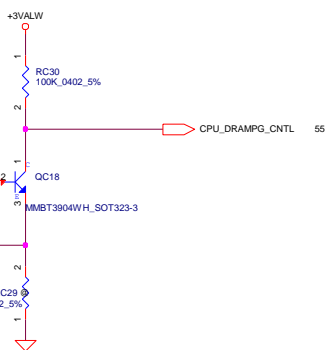
DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Full up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Full up to 3.3 V with 2.2Kohm	NC

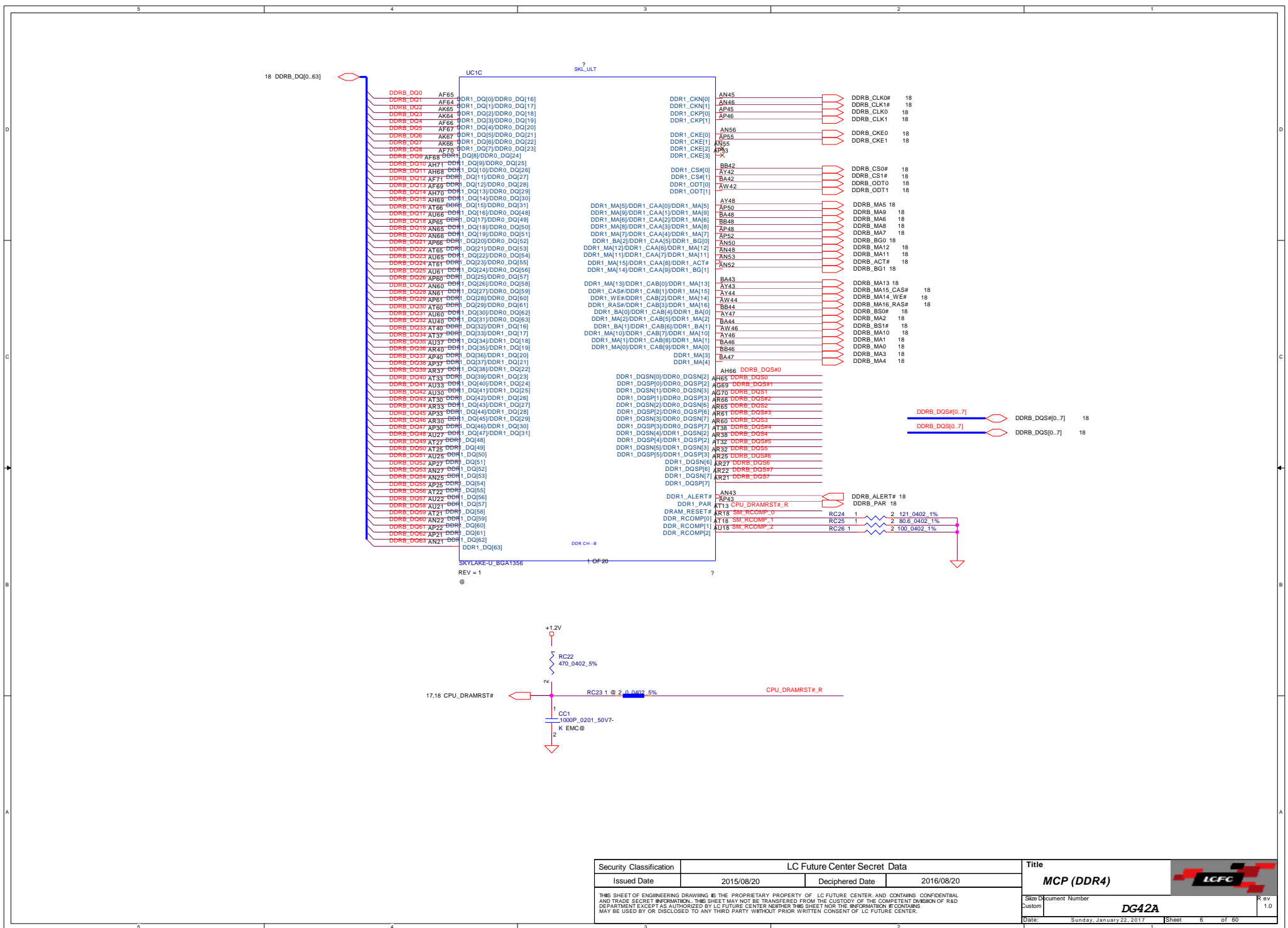


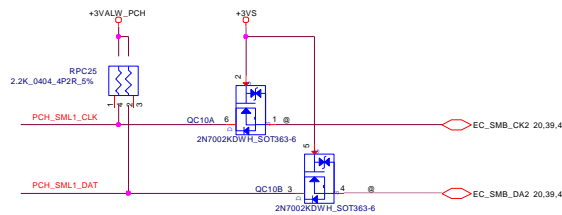
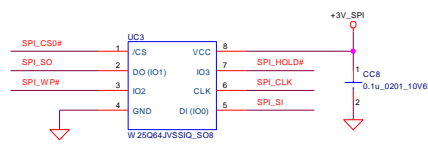
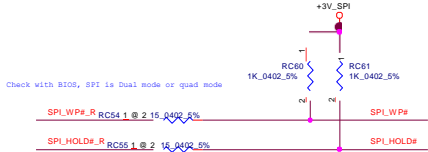
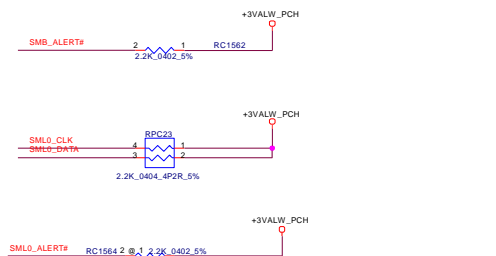
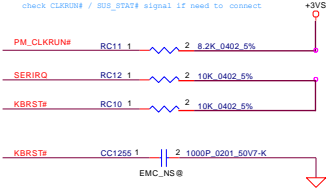
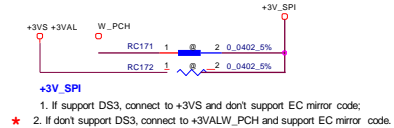
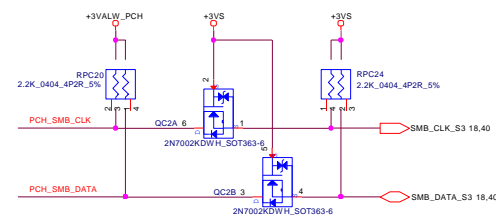
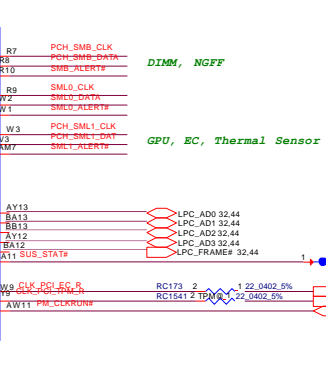
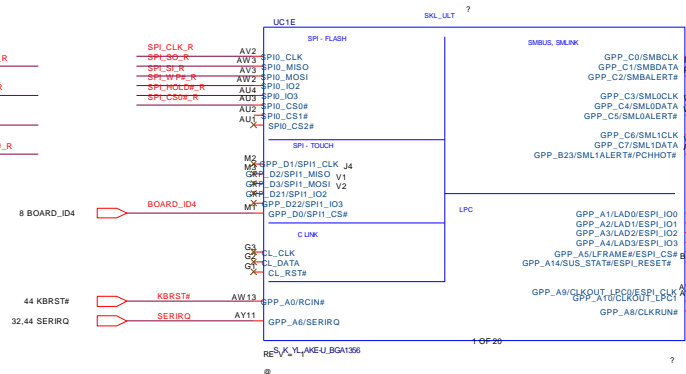
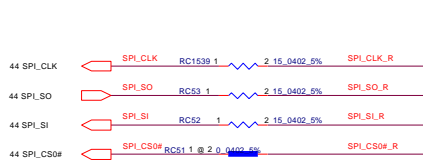


SKYLAKE-U, BGA1356
REV = 1
1 OF 20

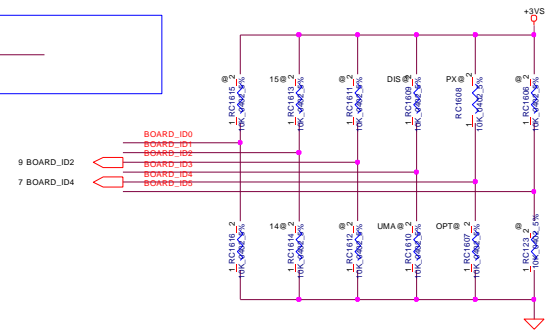


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				Custom	1.0
				DDG42A	
				Date	Sheet 5 of 60
				Sunday, January 22, 2017	



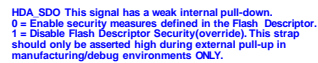


This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well Rising edge of RSMRST#



The schematic diagram illustrates the DIMM bus for the 16GB configuration. It features a 32-bit bus with 8 data lines (BOARD_ID6 to BOARD_ID13) and 24 address/strobe lines. The bus is terminated at both ends with 520Ω and 320Ω resistors. The schematic includes labels for DIMM_ONLY# and DIMM_ONLY@, and a 3VS power supply connection.

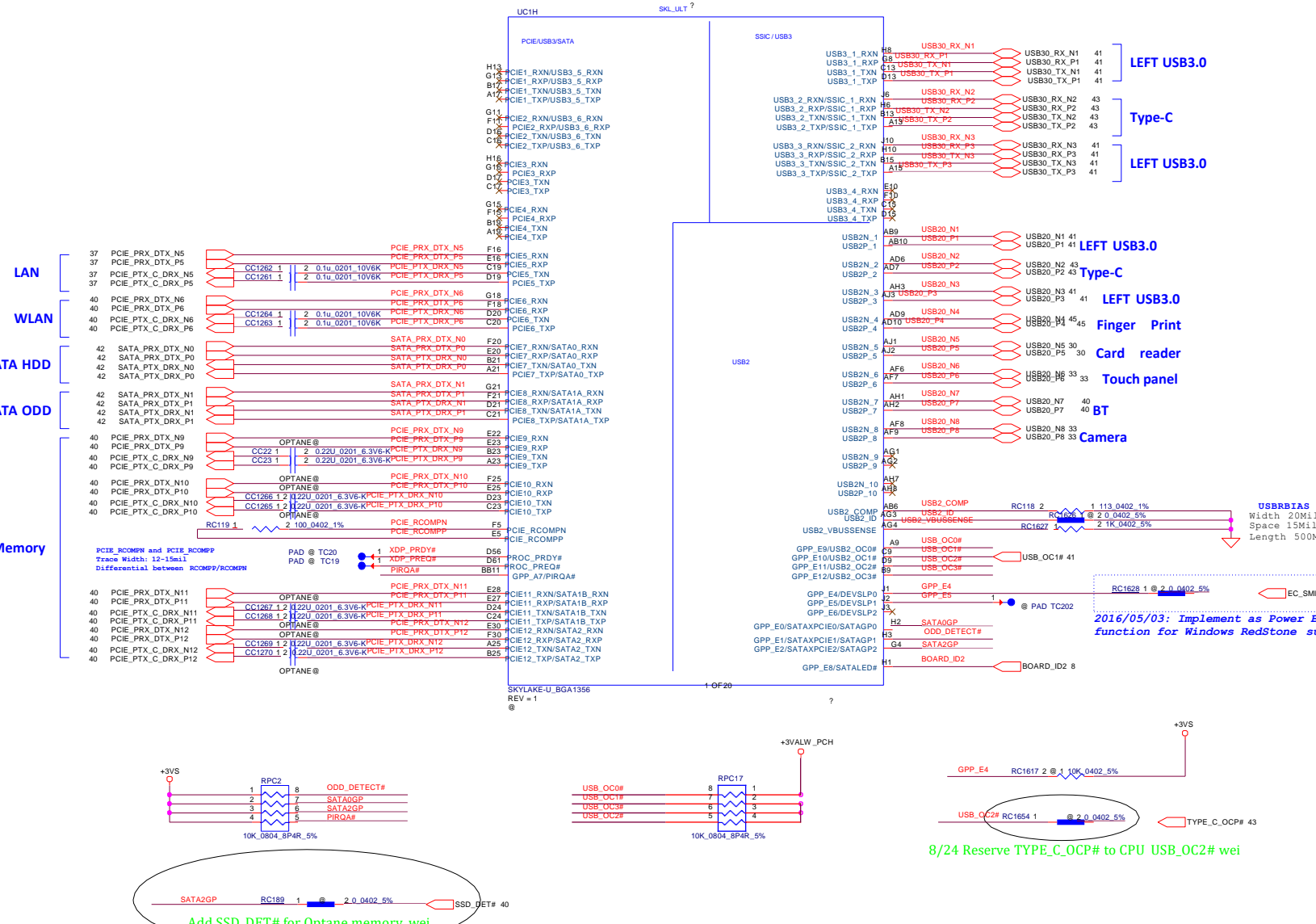
double check if need the pull-up resisor

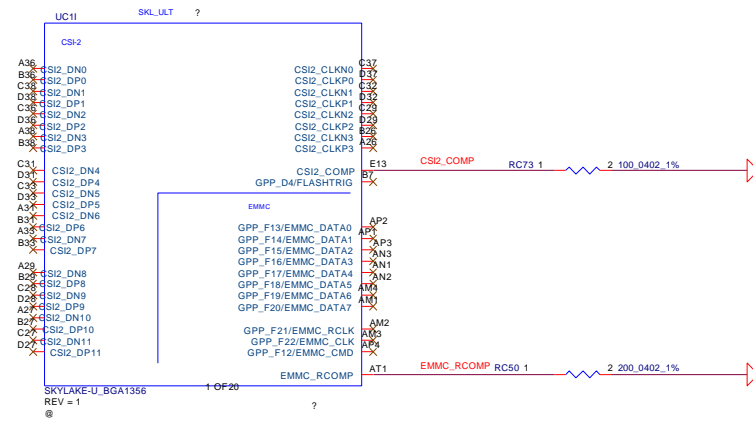
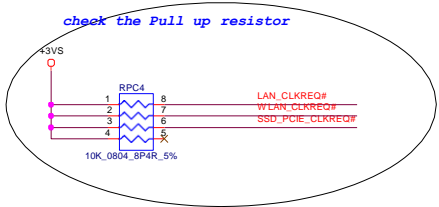


Pinmux diagram for SKYLAKE-U_BGA1356. The diagram shows connections for various pins and components. The components are labeled: UICG, AUDIO, SKL_UART7, and SDIO/SDXC. The pins are labeled: RC43_1, RC42_1, RC44_1, HDA_SYNC, HDA_BCLK, HDA_RST#, BOARD_ID0, BOARD_ID9, PCH_BEEP, GPP_0/G0/SD_CMD, GPP_1/G1/SD_DATA0, GPP_2/G2/SD_DATA1, GPP_3/G3/SD_DATA2, GPP_4/G4/SD_DATA3, GPP_5/G5/SD_CMD, GPP_6/G6/SD_CLK, GPP_7/G7/SD_WP, GPP_A17/SD_PWR_EN/HSH, GPP_A18/SD_1PR/SL, SD_RCOMP, GPP_F23, RC48, and RC49. The diagram also shows internal components like UICG, AUDIO, SKL_UART7, and SDIO/SDXC. The diagram is labeled with "1 OF 20" and "REV = 1".

Date:	Sunday, January 22, 2017	Sheet 8 of 60
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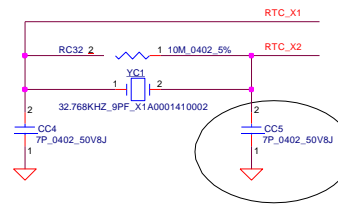
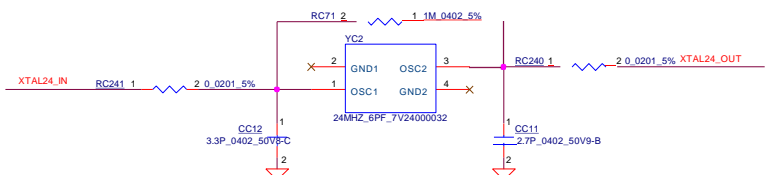
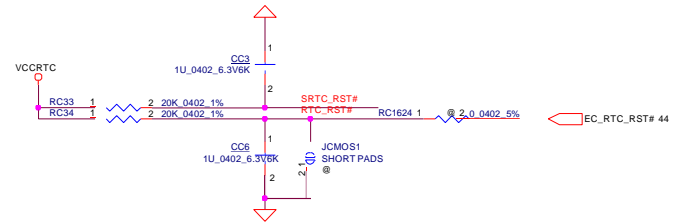
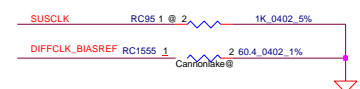
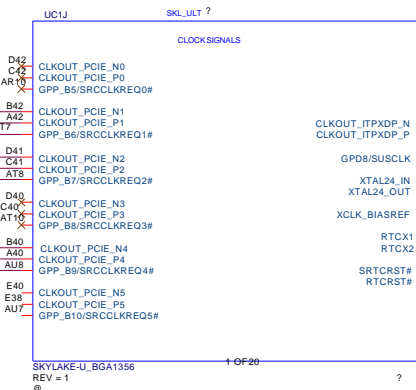


Optane memory

PCIE CLK5 WLAN

PCIE CLK4 LAN

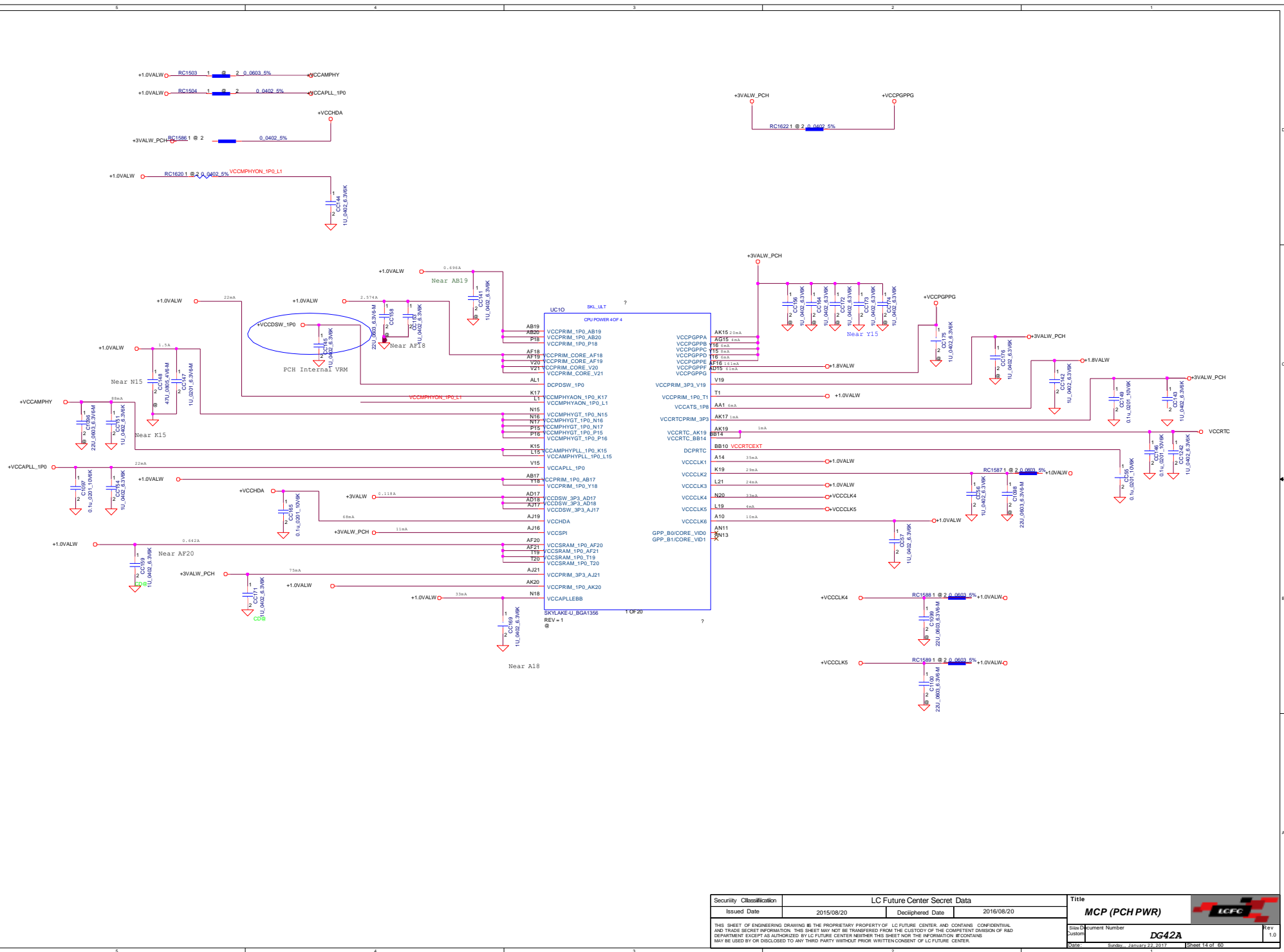
- 40 CLK_PCIE_SSD#
- 40 CLK_PCIE_SSD
- 40 SSD_PCIE_CLKREQ#
- 40 CLK_PCIE_WLAN#
- 40 CLK_PCIE_WLAN
- 40 WLAN_CLKREQ#
- 37 CLK_PCIE_LAN#
- 37 CLK_PCIE_LAN
- 37 LAN_CLKREQ#

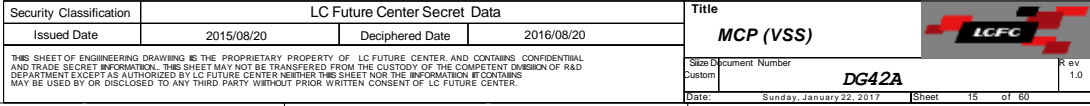


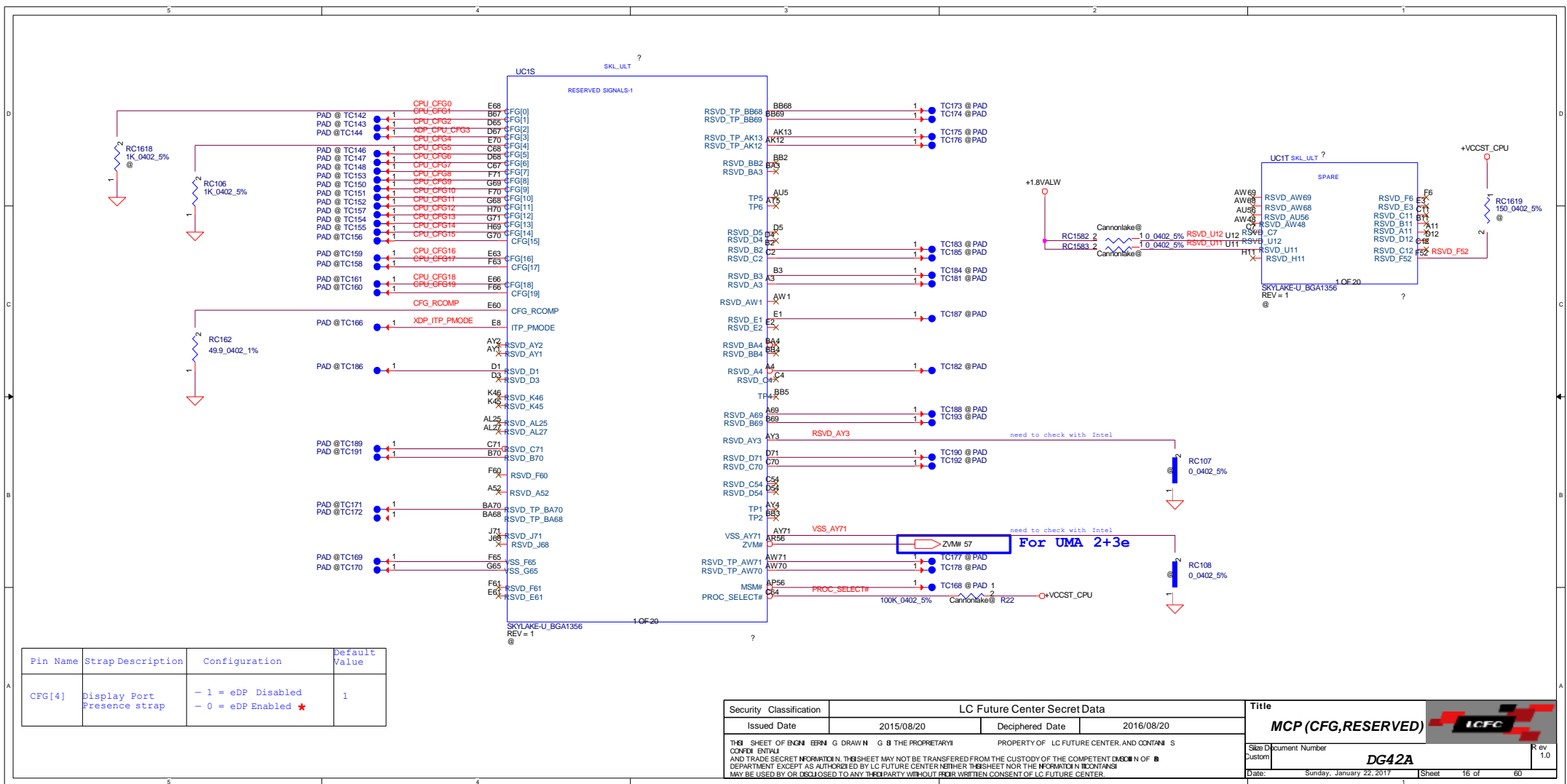
when single end external clock generator used, this pin should be grounded

need to use 38.4MHz (30ohm) for Cannonlake-u


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				Custom	1.0
				Date:	10 of 60
				Sunday, January 22, 2017	

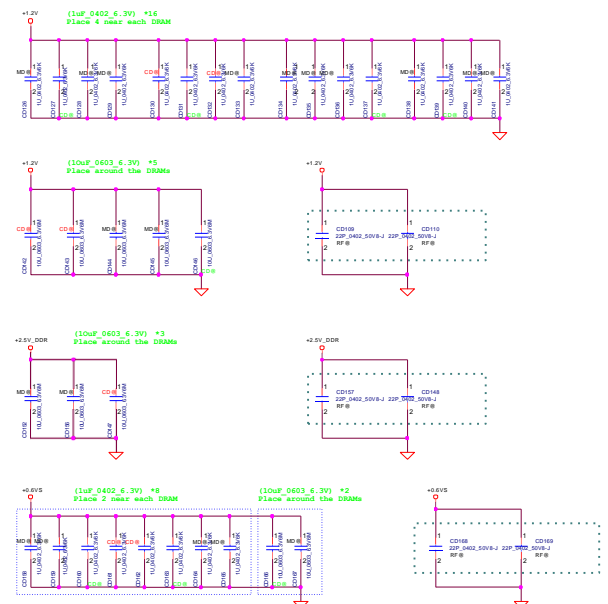


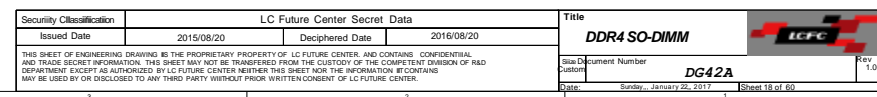


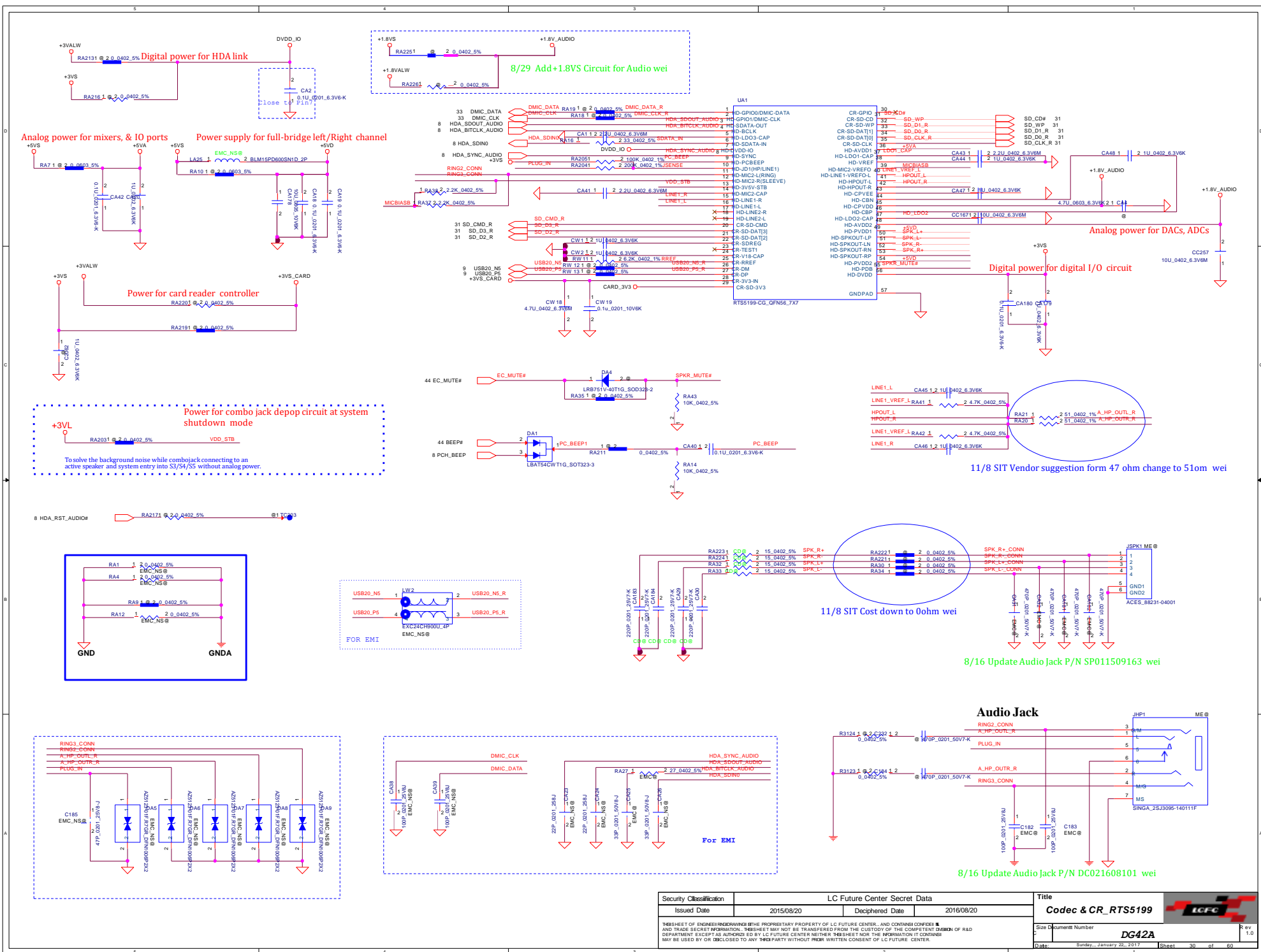


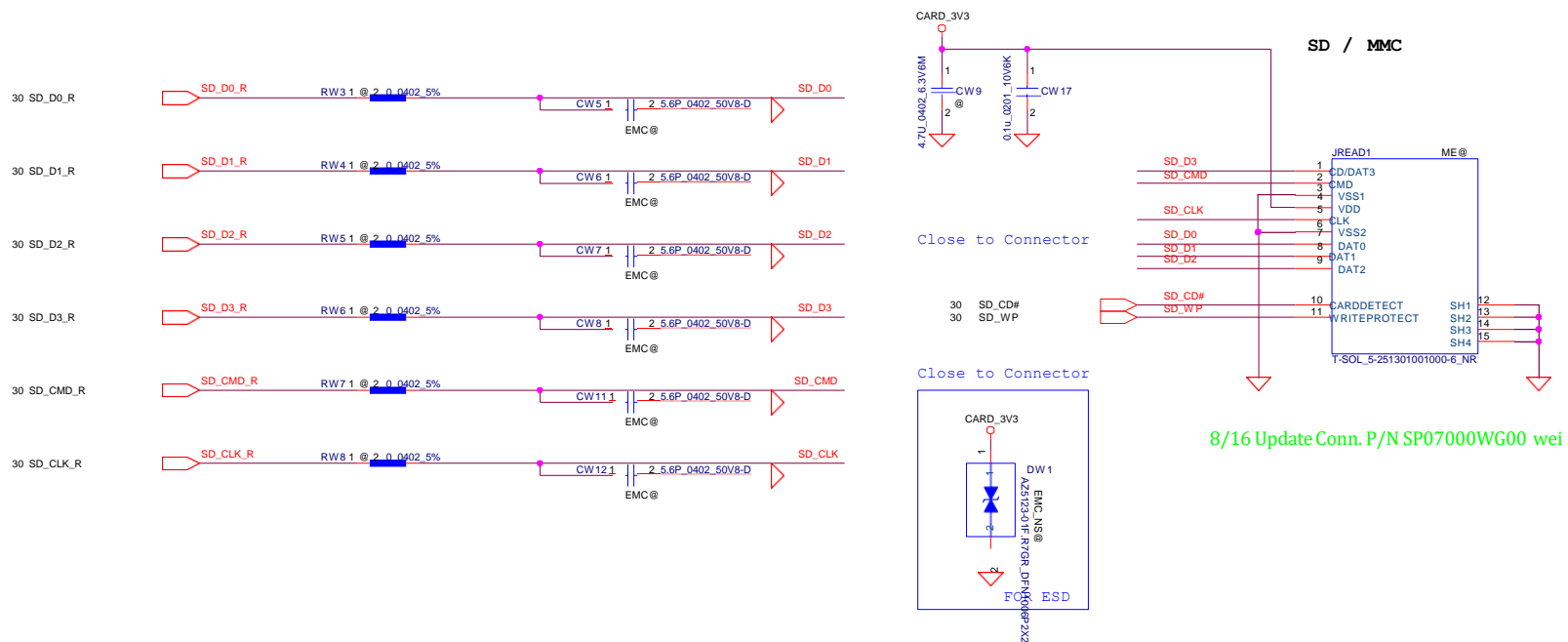
Pin Name	StrapDescription	Configuration	Default Value
CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled ★	1


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DATE: Sunday, January 22, 2017						Sheet 16 of 60		

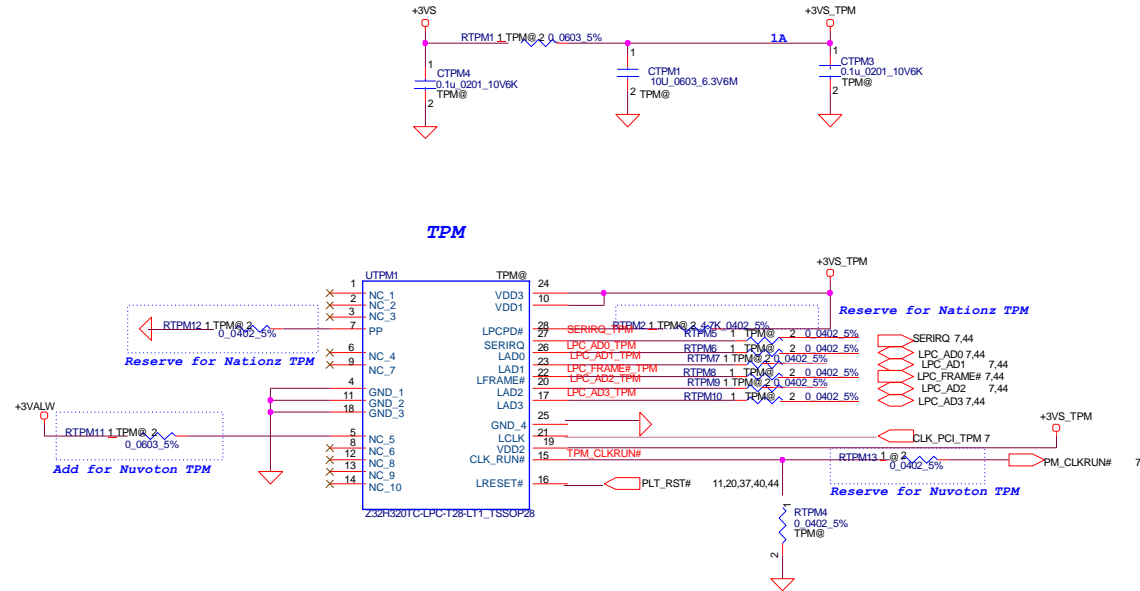








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Date: Sunday, January 22, 2017				Sheet 31 of 60 Rev 1.0



	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

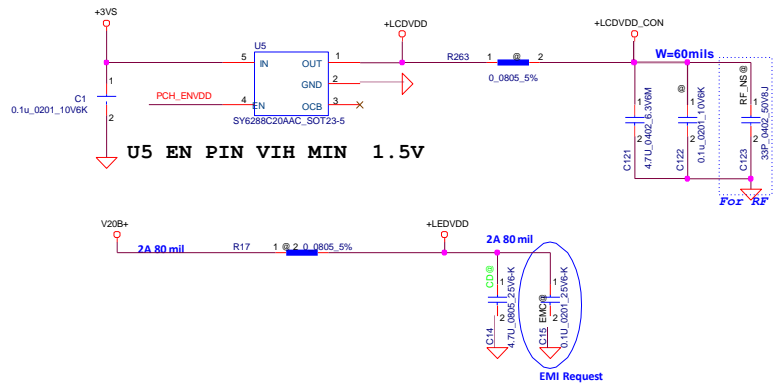
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Title	TPM		
Site Document Number	DG42A		
Date	Sunday, January 22, 2017	Sheet	32 of 60

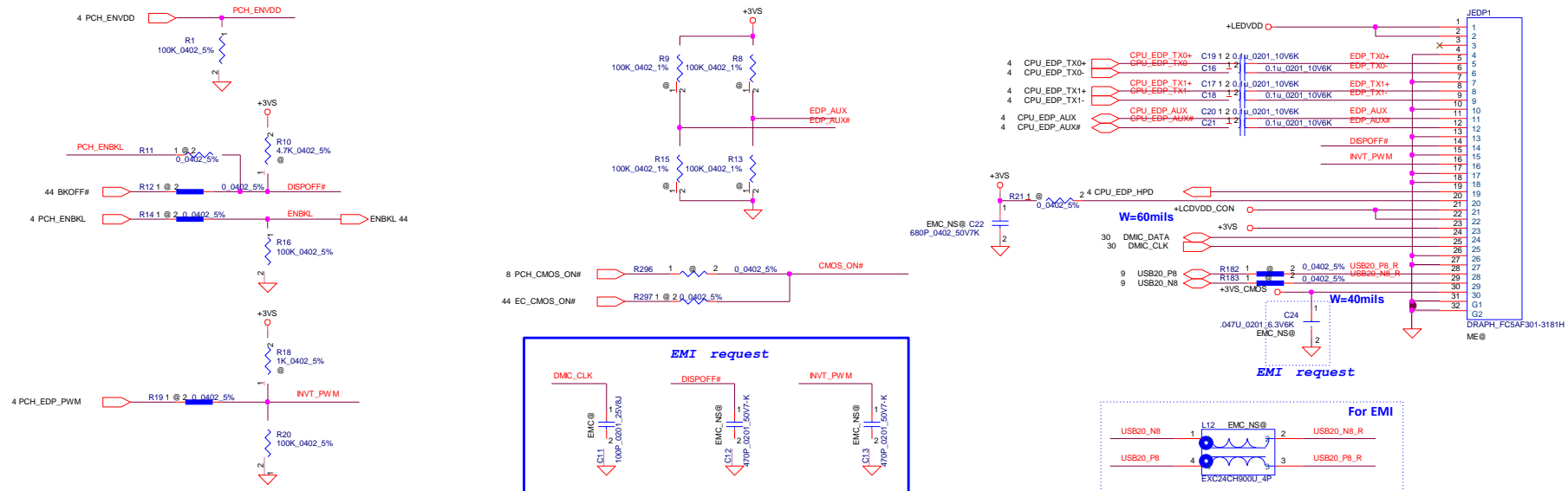
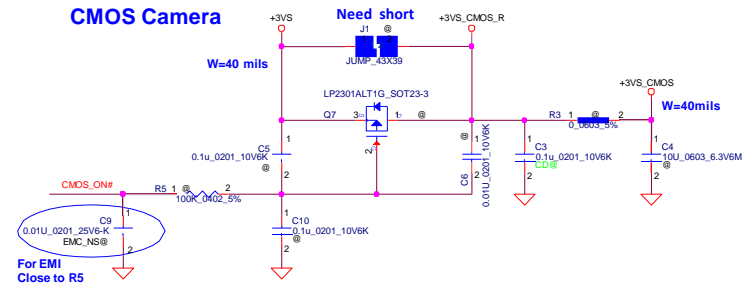


Rev 1.0

LCD POWER CIRCUIT

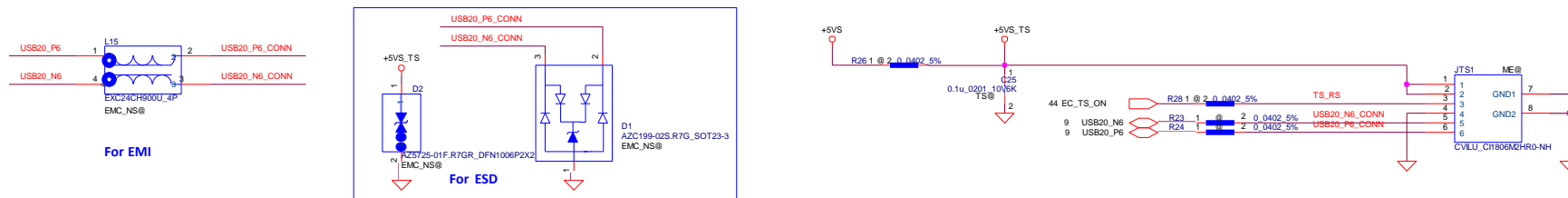


CMOS Camera

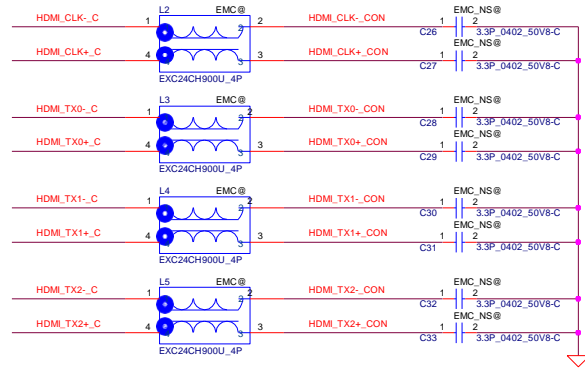


Touch Screen

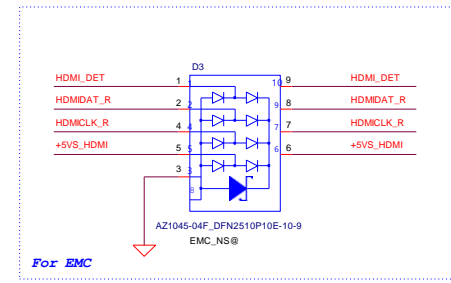
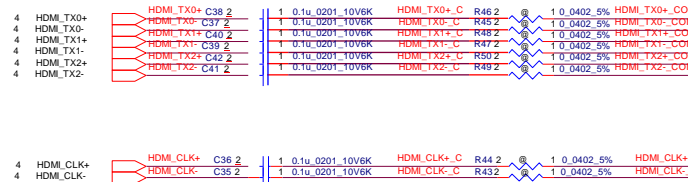
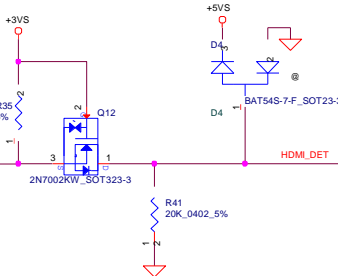
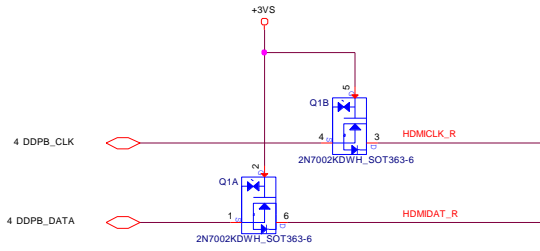
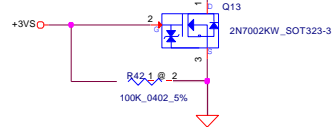
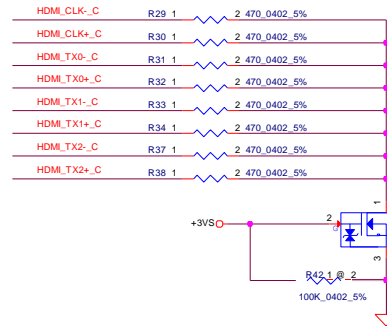
Touch Screen



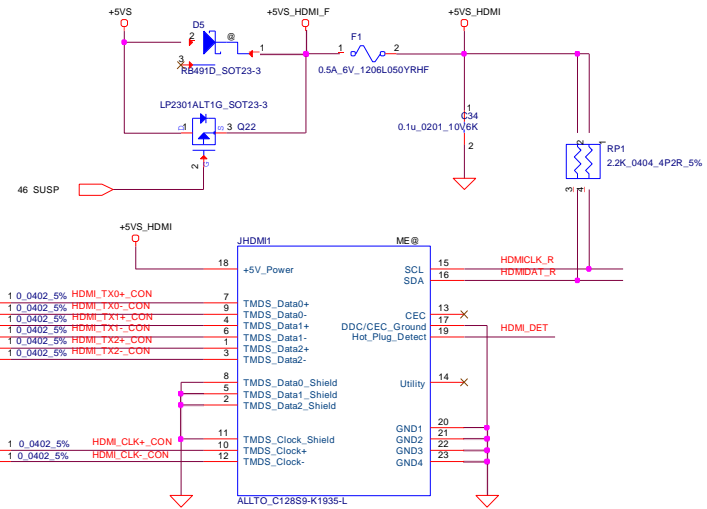
Security Classification	LC Future Center Secret Data		Title	eDP/CMOS/Touch screen	
Issued Date	2015/08/20	Doc#	ered Date	2016/08/20	
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Size/Doc Number	Custom		Rev	1.0	
Date	Sunday, January 22, 2017		Sheet	33 of 60	



For EMC

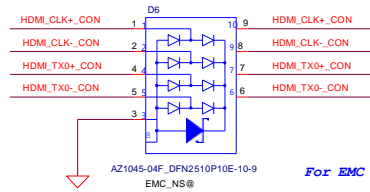


For EMC

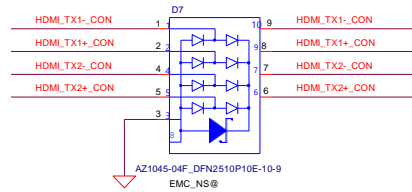


8/16 Update HDMIConn.P/N DC021608081wei


Close to JHDMI1



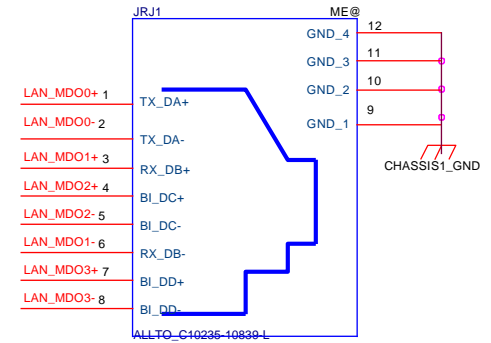
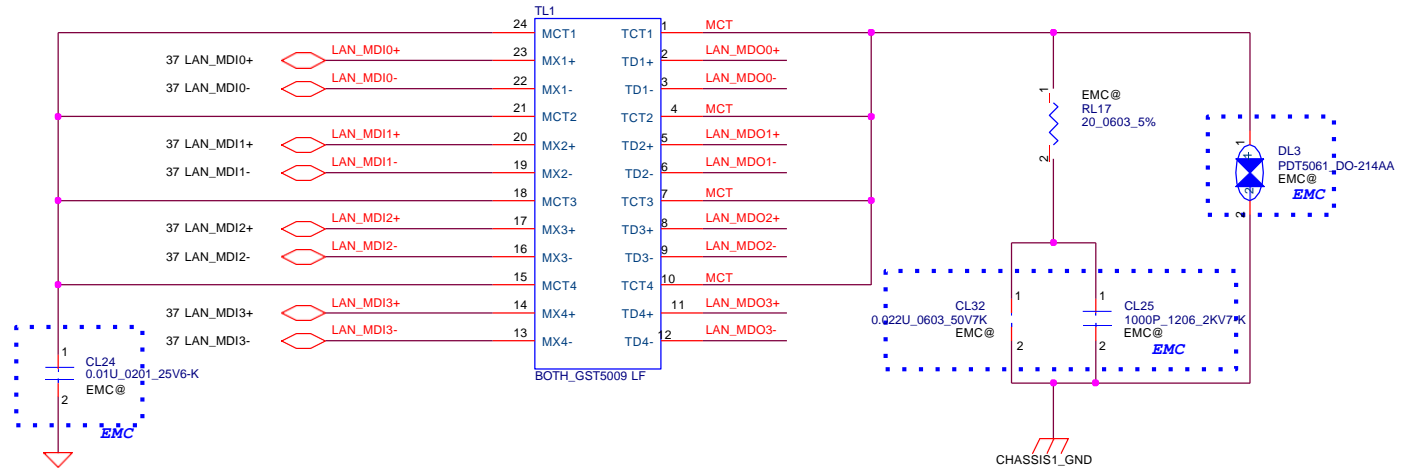
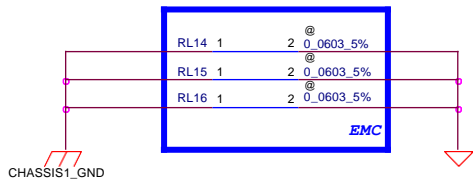
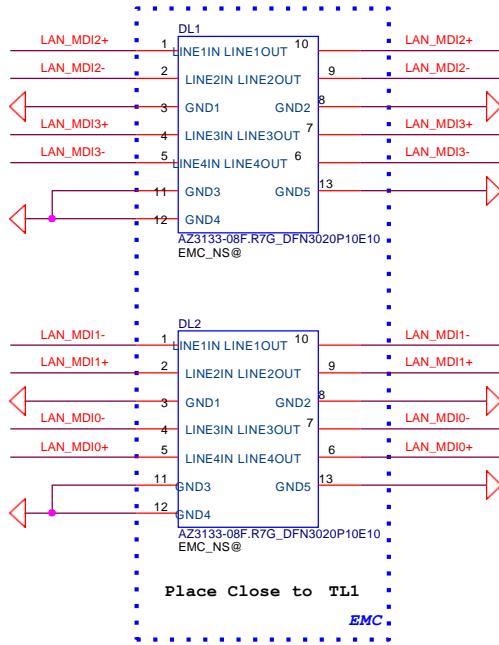
For EMC



For EMC

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	HDMI_CONN	
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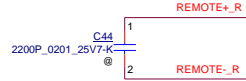
DL1/DL2
1'S PN:SC300003M00



8/16 Update RJ45 P/N DC021608091 wei

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_Transformer	
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				DG42A	1.0
Date:		Sunday, January 22, 2017		Sheet	38 of 60

Close to U1

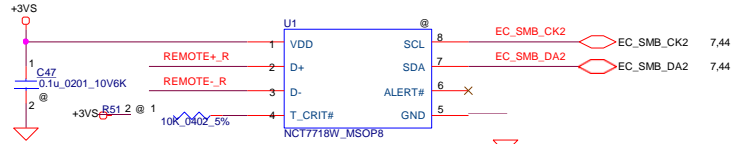


REMOTE+_R R176 1 @ 2 0.0402 5% REMOTE2+

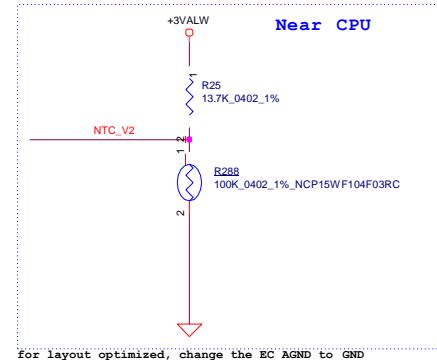
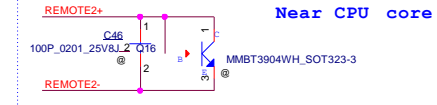
REMOTE-_R R177 1 @ 2 0.0402 5% REMOTE2-

REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

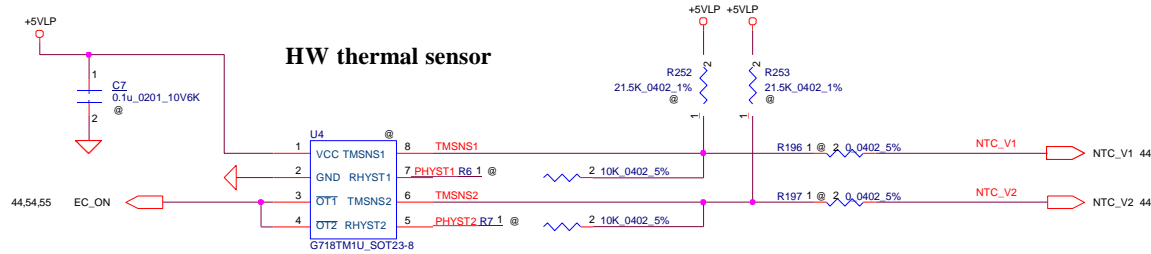


Address 1001_101xb



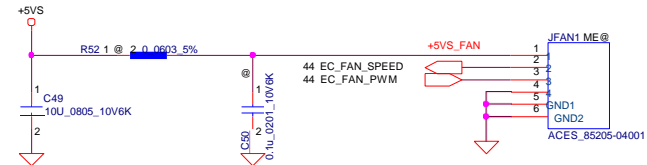
for layout optimized, change the EC_AGND to GND

HW thermal sensor



over temperature threshold:
 $RSET=3*RTMH$
 $92\pm 30C$
Hysteresis temperature threshold:
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $56\pm 30C$

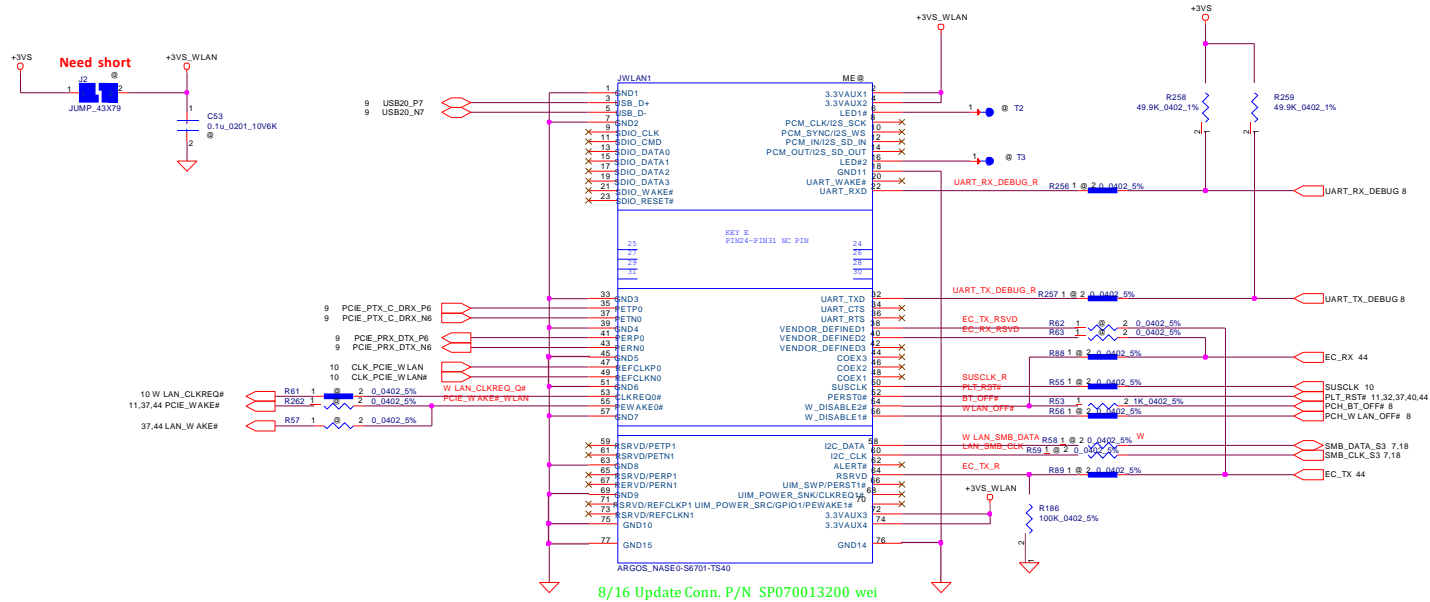
FAN Conn



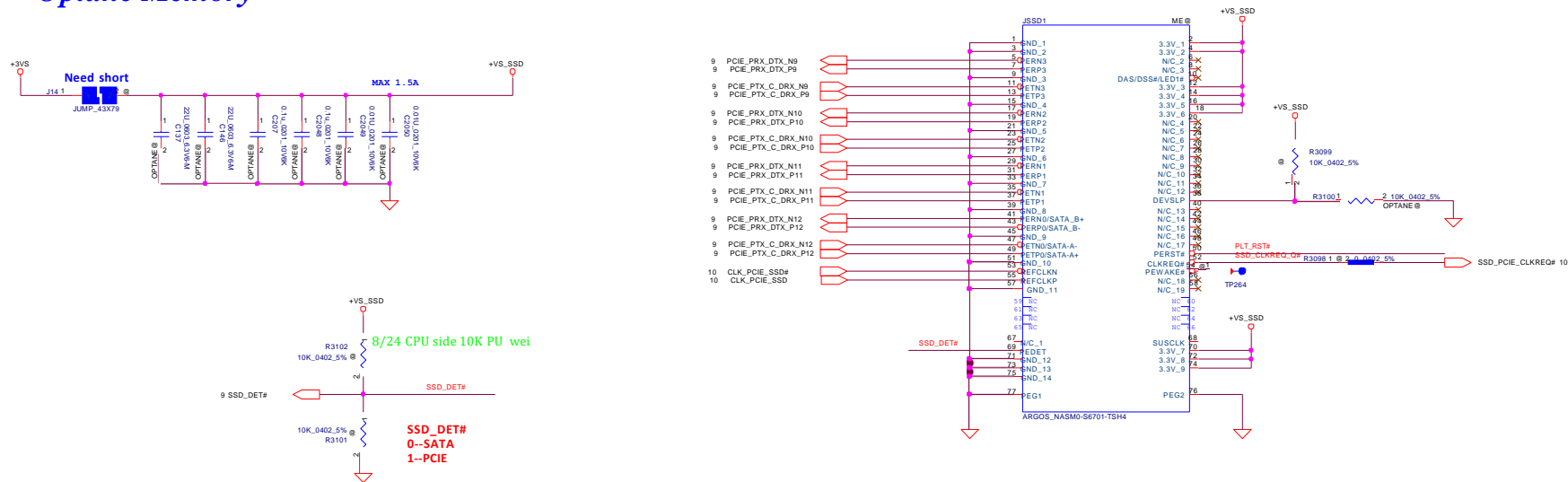
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20
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Title		Thermal sensor/FAN Conn	
Size	Document Number	DG42A	
Custom		1.0	
Date:	Sunday, January 22, 2017	Sheet	39 of 60

Mini-Express Card(WLAN/WiMAX)

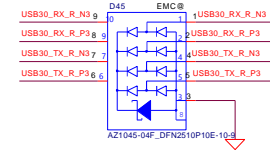
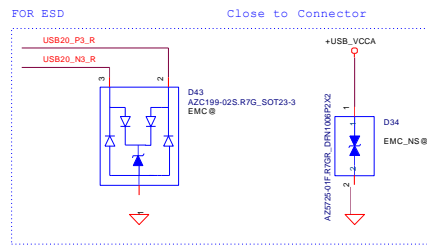
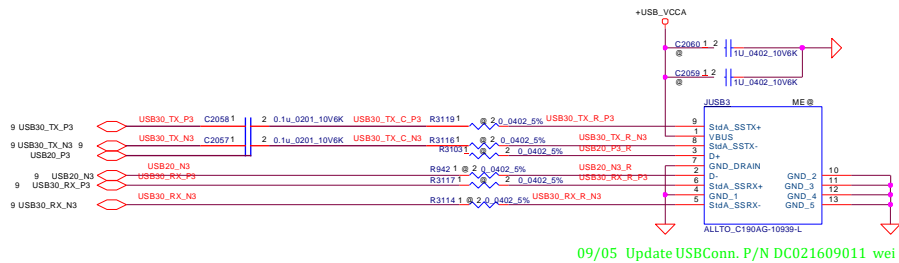
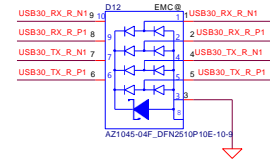
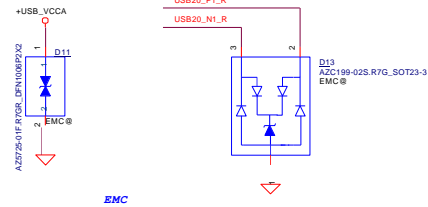
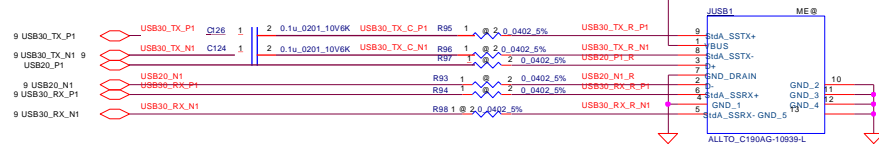
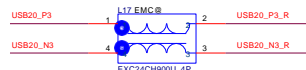
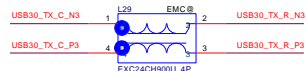
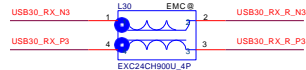
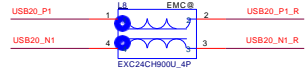
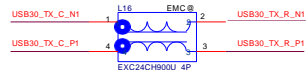
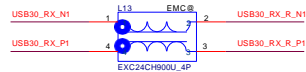
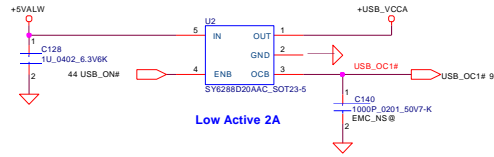


Optane Memory



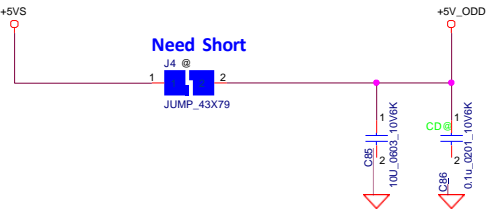
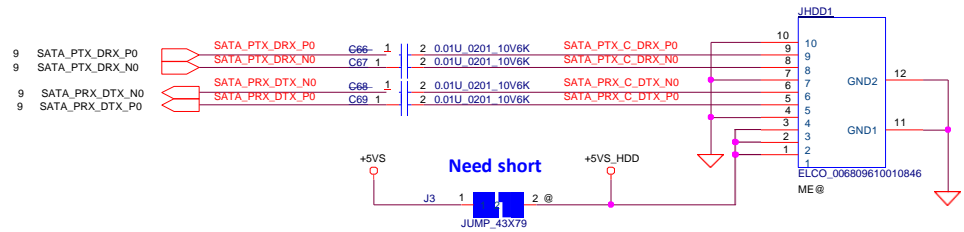
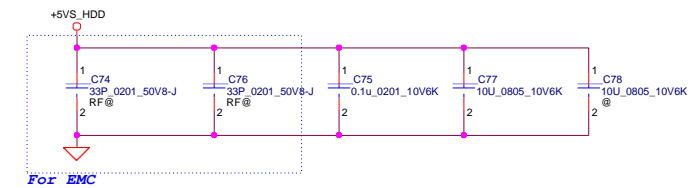
Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		NGFF WLAN&SSD			
2015/08/20		2016/08/20		Size Document Number C		Rev	
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Date:				Sunday, January 22, 2017		Sheet 40 of 60	

LEFT SIDE USB3.0 PORT x2

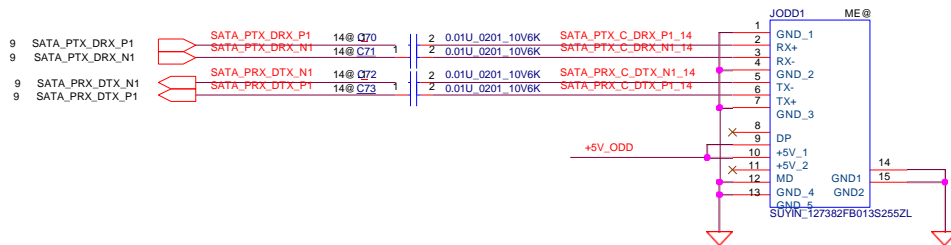


Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		USB3.0 PORT (LEFT)	
2015/08/20		2016/08/20		Size Document Number C	
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				Sheet 41 of 60	

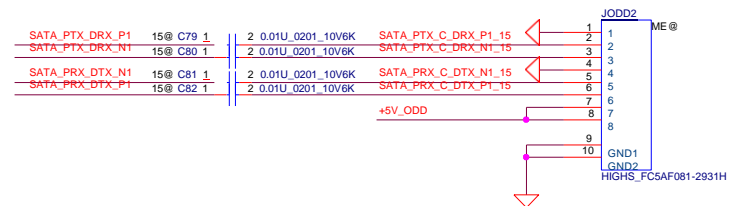
SATA HDD Conn.




FOR 14" SATA ODD Conn.

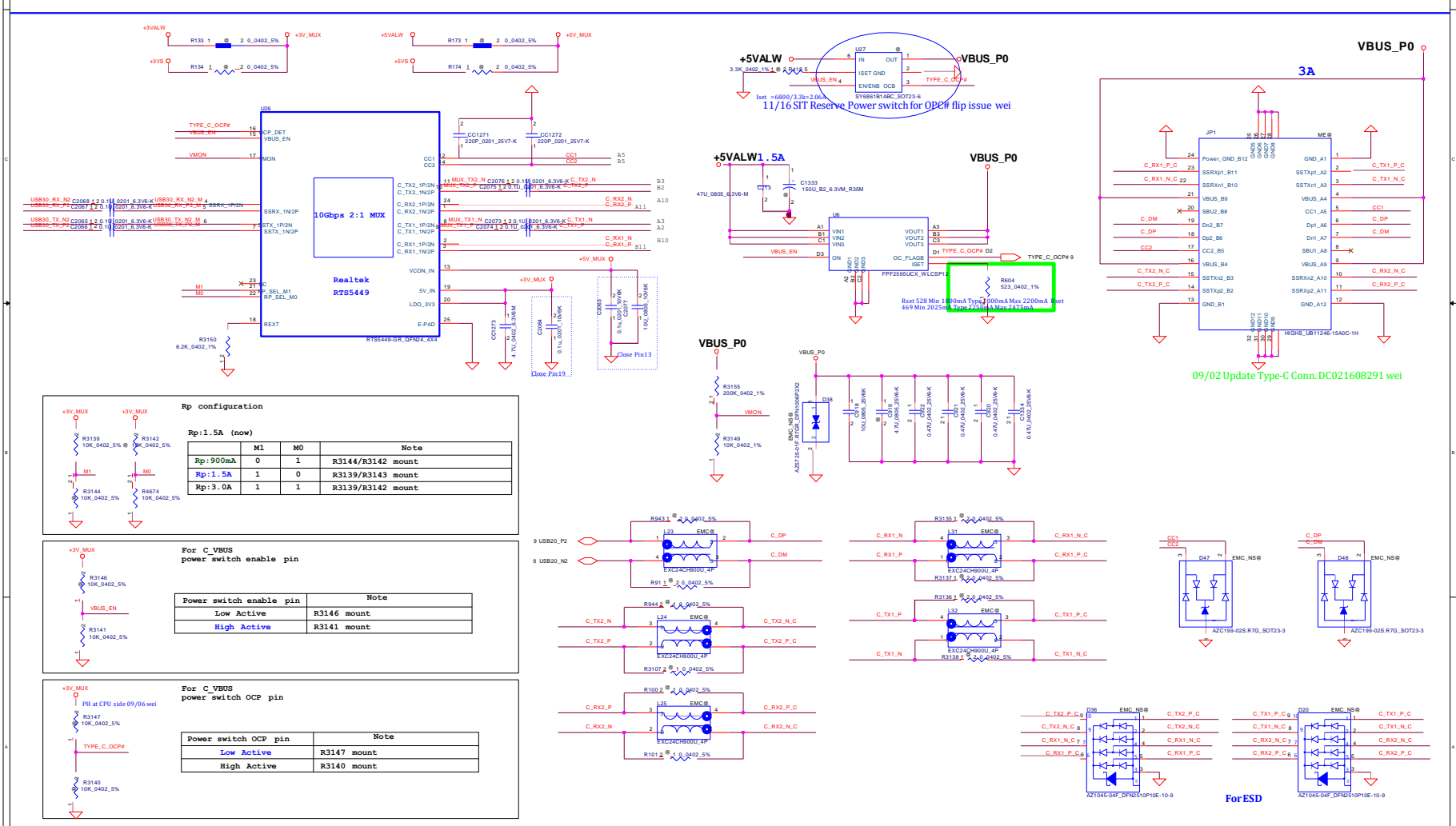


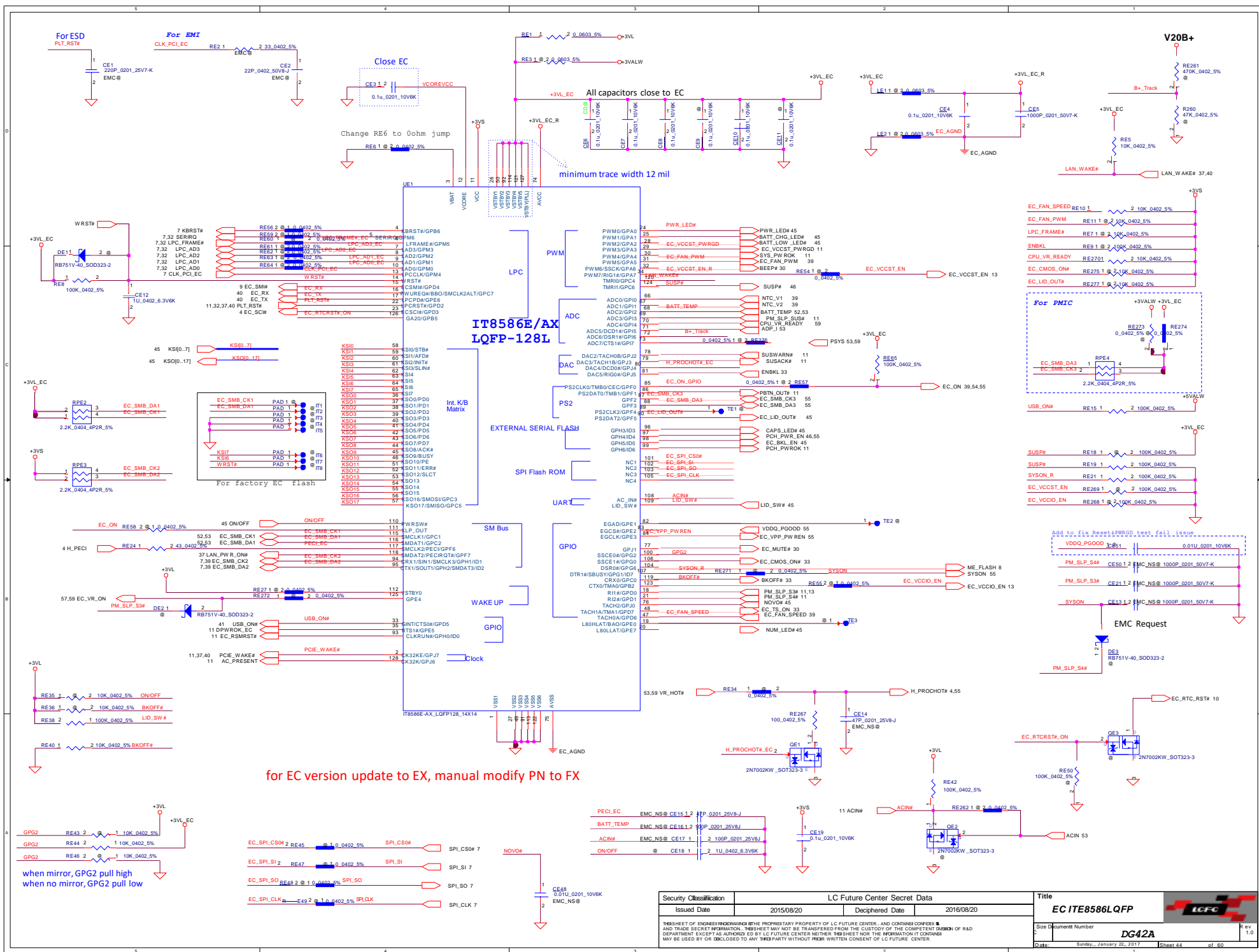
FOR 15" 17" SATA ODD FFC Conn



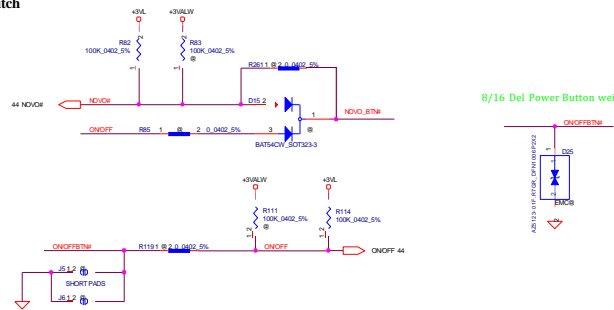
8/16 Update Conn. P/N SP01001YV00 wei

Security Classification		LC Future Center Secret Data		Title		
Issued Date		2015/08/20	Deciphered Date	2016/08/20	HDD/ODD CONN	
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Size		Document Number		Custom		Rev
				DG42A		1.0
Date:		Sunday, January 22, 2017		Sheet		42 of 60

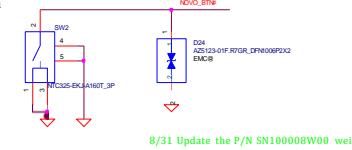
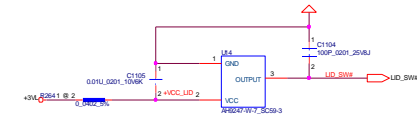




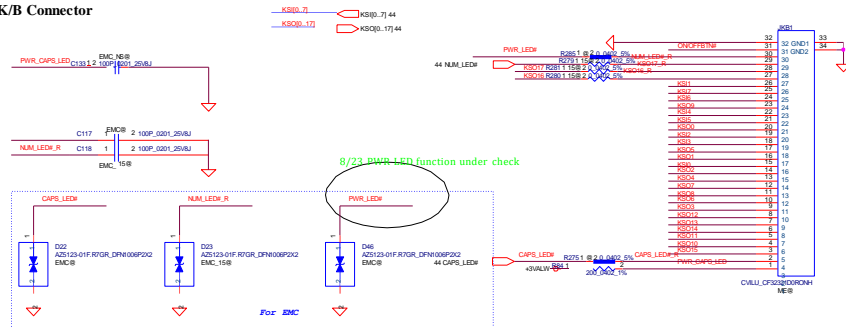
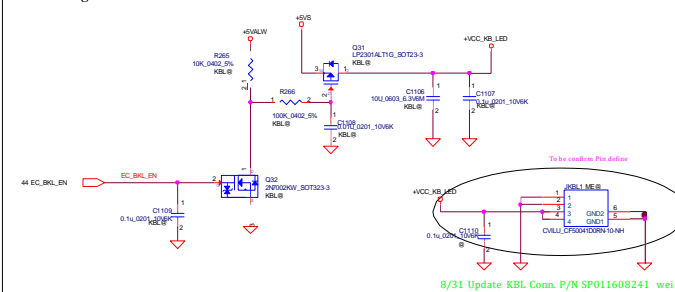
ON/OFF switch



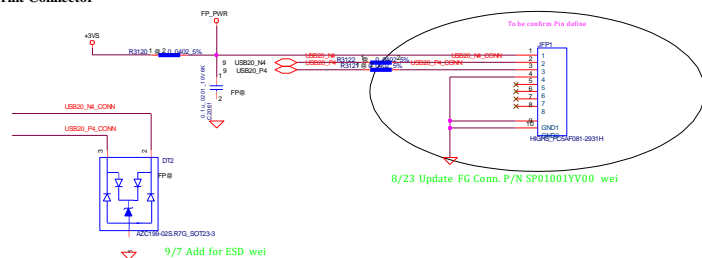
Novo button

**LID switch**

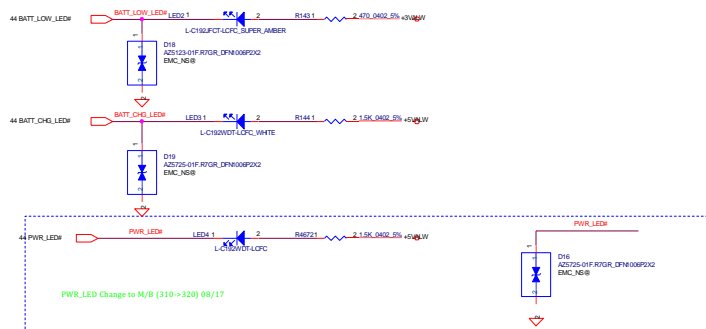
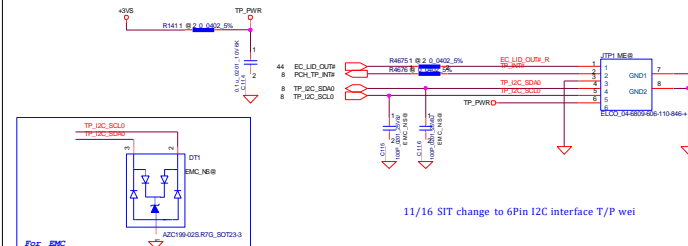
K/B Connector

**KB Backlight Connector**

Finger Print Connector



TP/B Connector



Security: Classified only	LC Future Center Secret Data		Title
Issued Date	2015/05/20	Declassified Date	2016/08/20
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Doc Number/Serial Number			DG42A

Load Switch
+5VALW To +5VS
+3VALW To +3VS

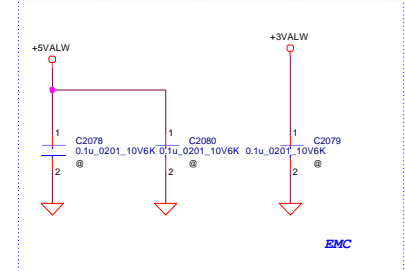
+3VS, C173 --> 2.74ms
+5VS, C176 --→ 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

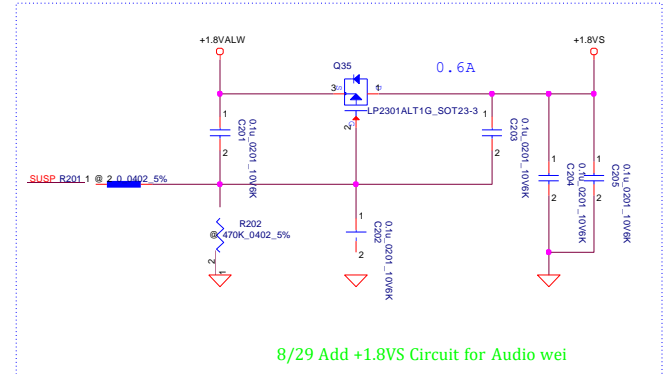
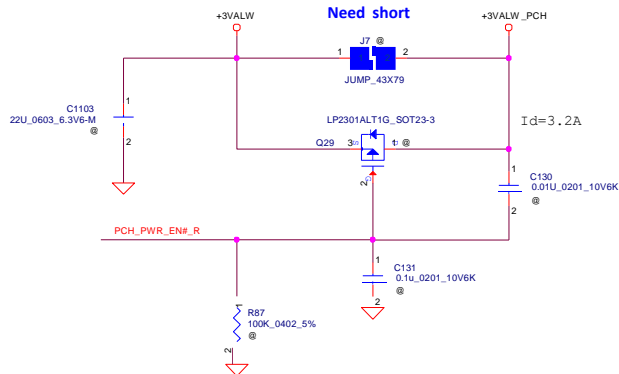
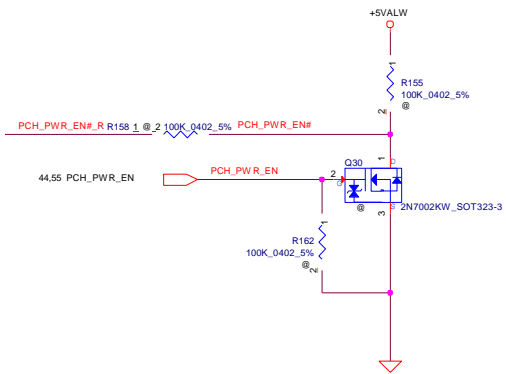
Need Short

Need Short

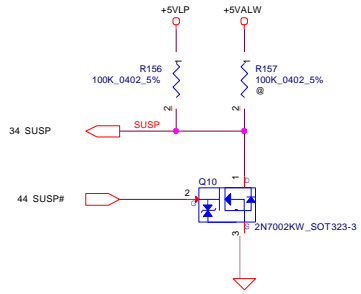
Change the main source to SA000067600 (GMT) 7/16



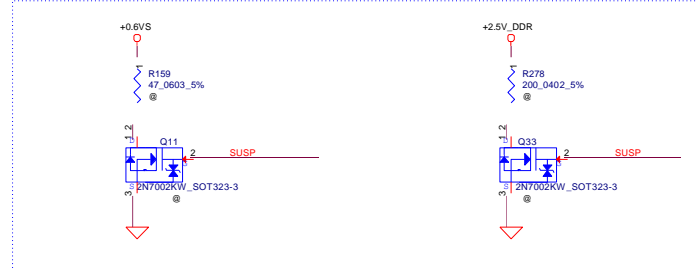
EMC





8/29 Add +1.8VS Circuit for Audio wei

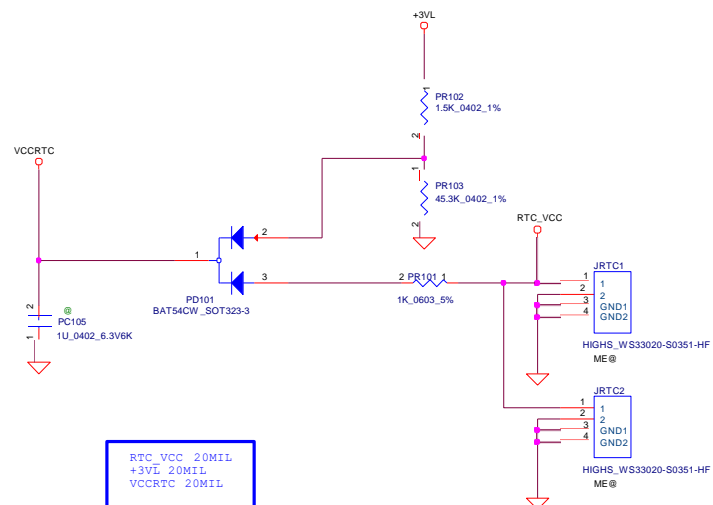
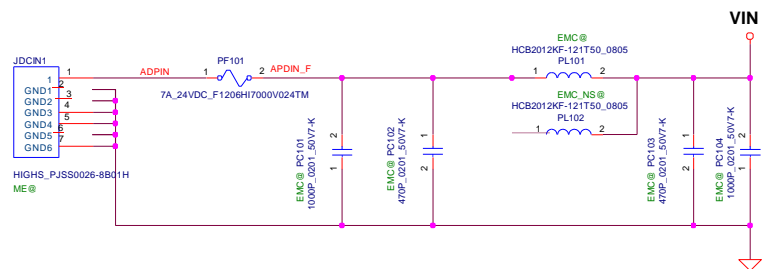


For DisCharge



08/29: Need double check enable signal and the resistance

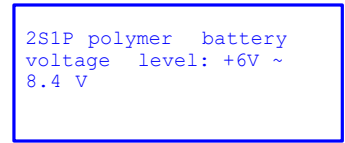
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	DC V to VSINTERFACE	
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				Custom	
				Date: Sunday, January 22, 2017	Sheet 46 of 60




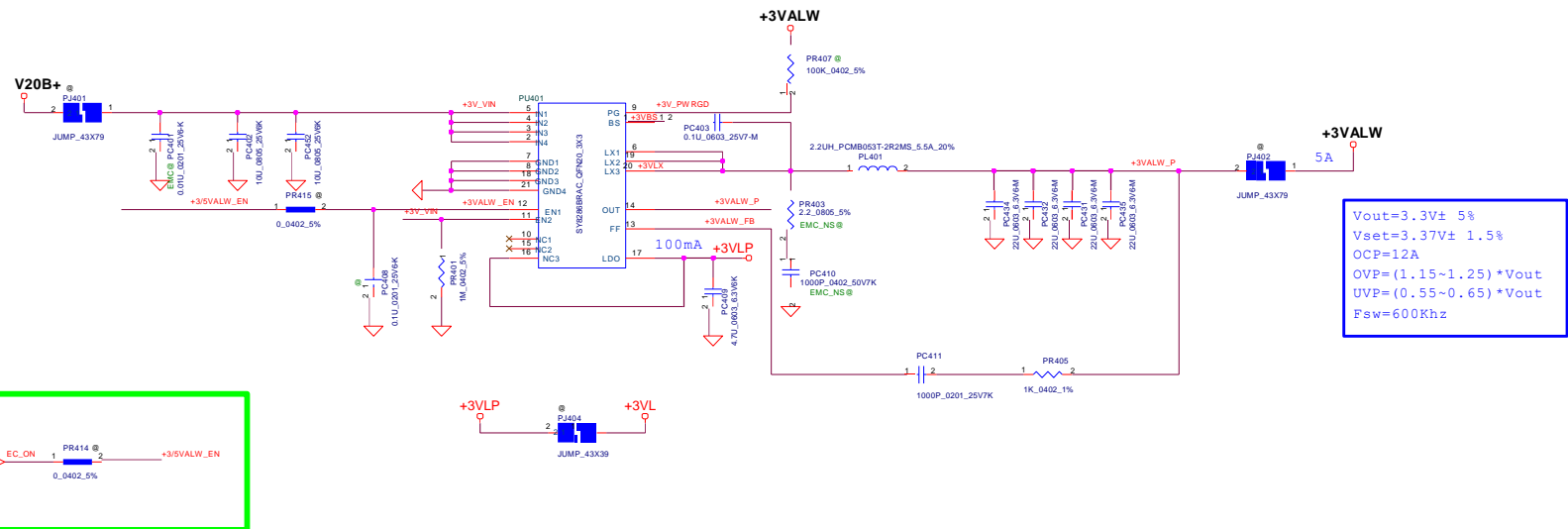
RTC VCC 20MIL
+3V_L 20MIL
VCCRTC 20MIL

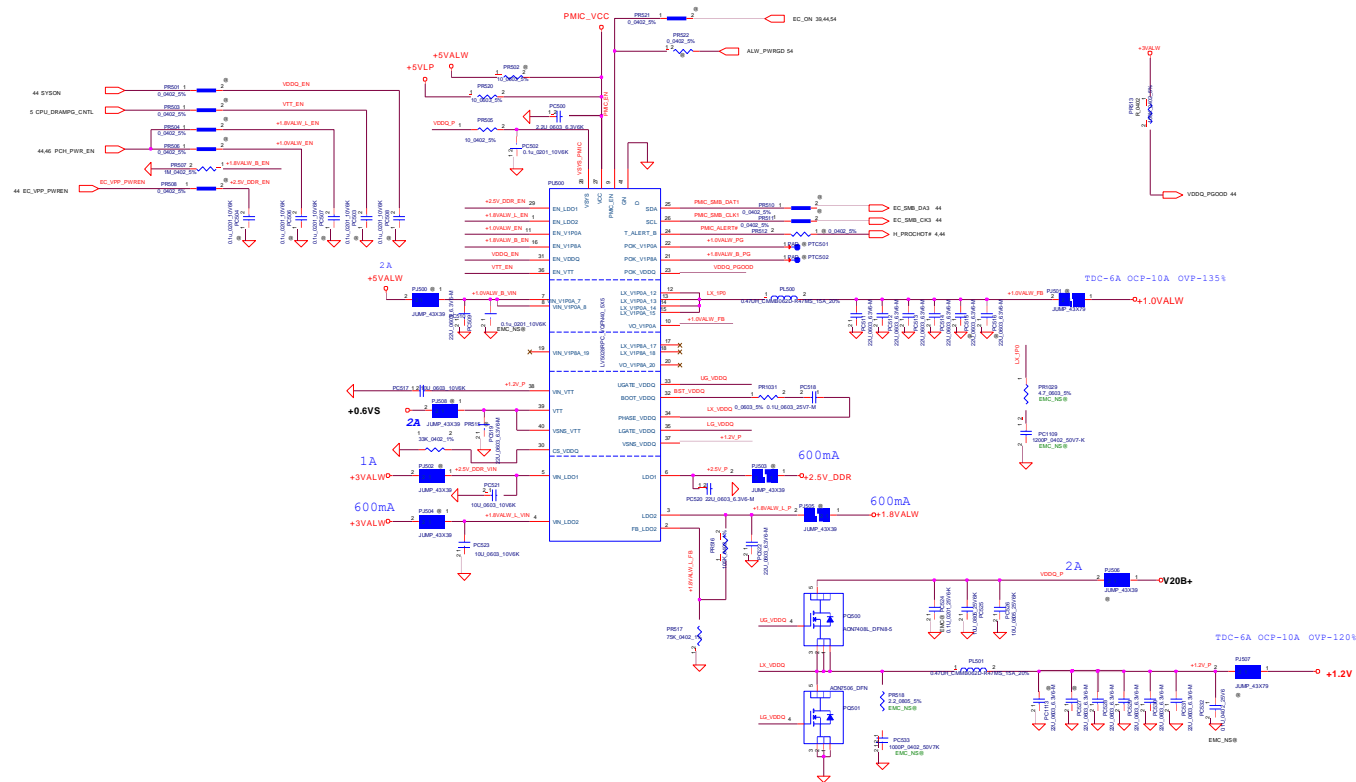
No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)

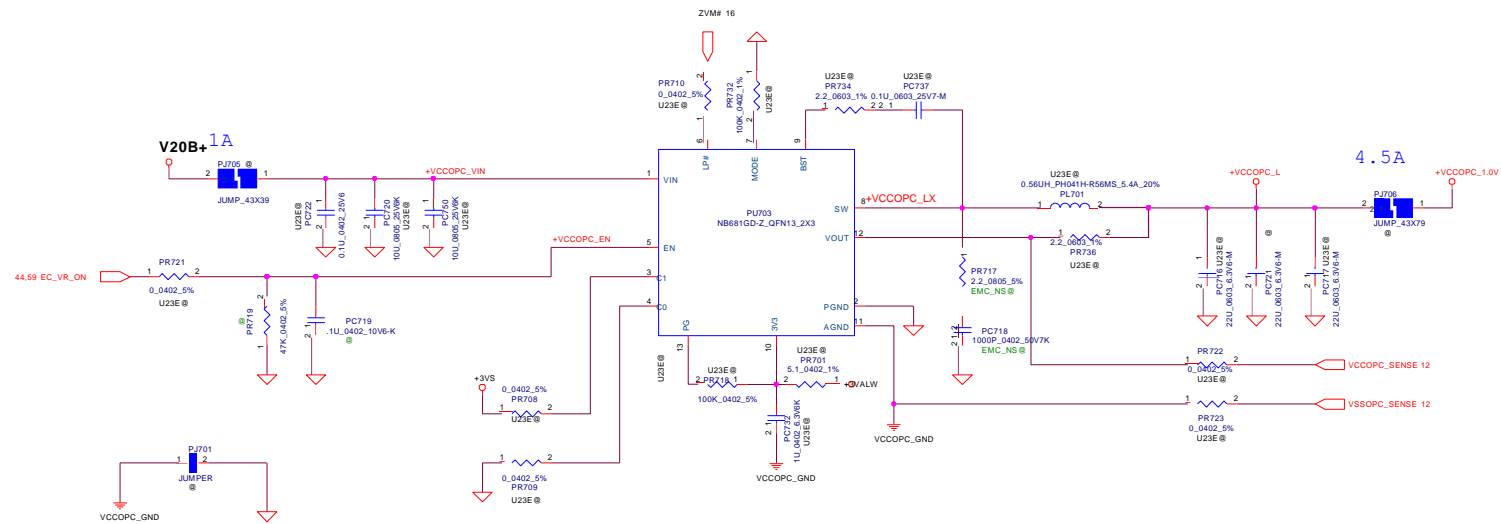
Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-DCIN / RTC charger
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				Date: Sunday, January 22, 2017 Sheet 51 of 60



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-BATTERY CONN/OTP	
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				Date: Sunday, January 22, 2017	Sheet 52 of 60



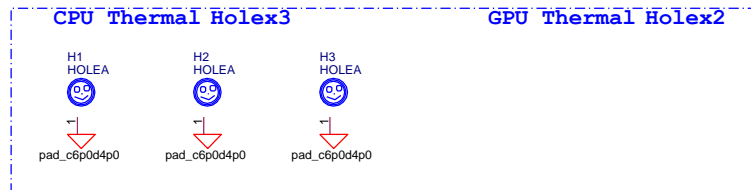




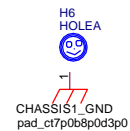
Security Classification		LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date	2016/08/20
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Title		PWR+VCCOPC	
Size	Document Number C	Rev	1.0
Date	Sunday, January 22, 2017	Sheet	57 of 60





Close to RJ45



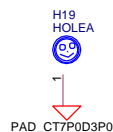
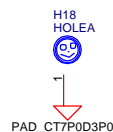
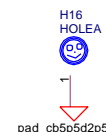
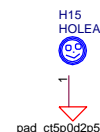
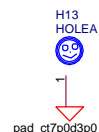
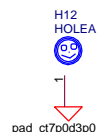
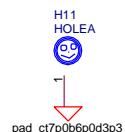
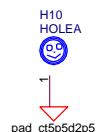
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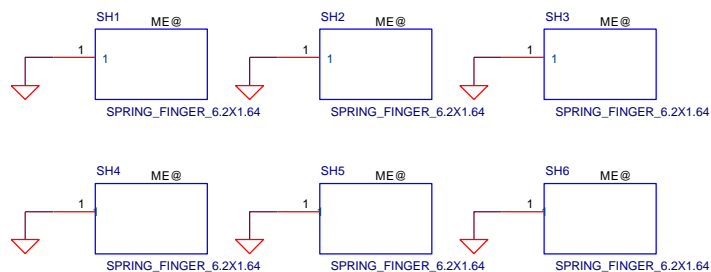
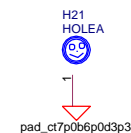
PCB Federal Mark PAD



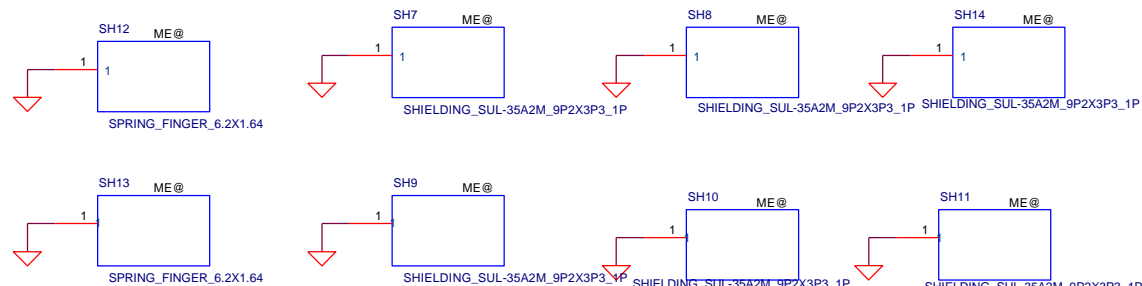
WLAN Standoff



Optane Standoff



USB3.0 Shielding



DDR4 Shielding

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Hole	
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				DG42A	1.0
				Date:	Sheet
				Sunday, January 22, 2017	49 of 60